FASTER QDC-TDC MnM USER MANUAL

This document is the user manual of the FASTER QDC-TDC module, called QDC-TDC MnM (**M**easurement **n**umerical **M**odule). The QDC-TDC MnM measures integrated charges in user-defined gates, and timestamps every event with a high accuracy.

In chapter one, you will find an introduction to the charge measurement chain and the time measurement chain.

In chapter two, all tuning parameters of the QDC-TDC MnM are described.

In chapter three, a QDC-TDC MnM tuning procedure is suggested.

Cathy Fontbonne

Cathy Fontbonne

Summary

I Theory of operation

I.A Elements of Charge Measurement

A QDC instrumentation chain is designed for radiation charge measurement. This system includes the essential modules shown in Figure 1.

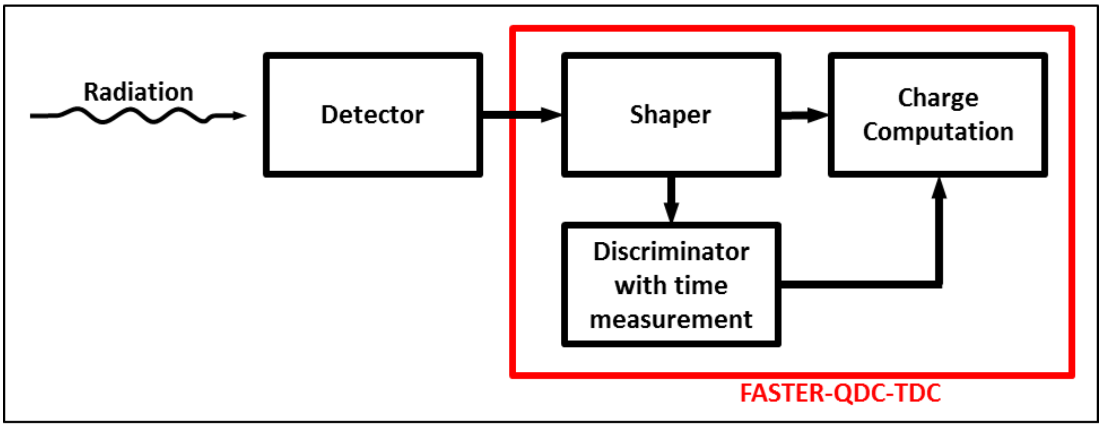

Figure 1: The essential modules in a QDC set-up.

In general, the QDC chain is used with self-amplified detectors (photomultiplier, Gas Electro Multiplier, Proportional Counters...). In the QDC-TDC MnM, the signal from the detector is immediately digitalized. Therefore, the signal processing is digital in FASTER-QDC-TDC.

I.B Elements of Time Measurement

The acquisition of FASTER is able to perform energy measurements using time of flight. Every QDC-TDC MnM operates in a synchronous way, and all the events are precisely time-stamped with the same reference. The user can then display the TOF measurement by using RHB features.

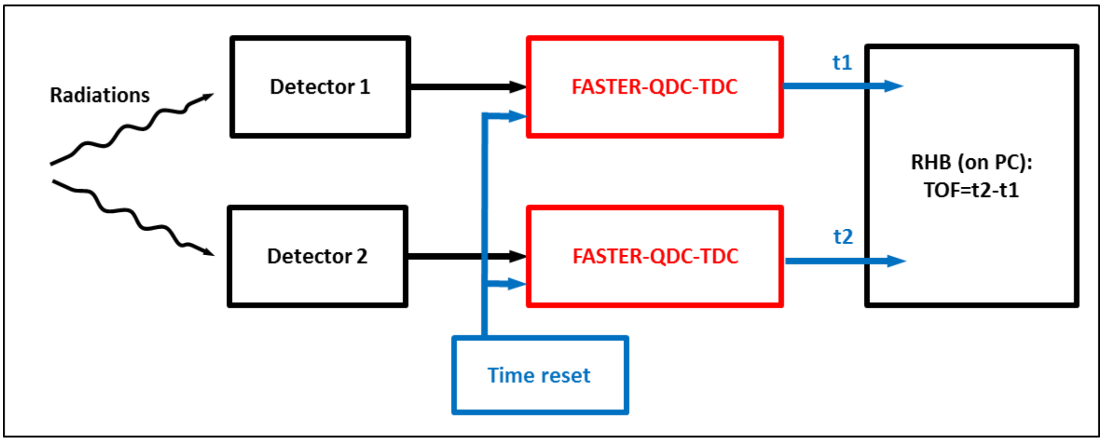

Figure 2: Time of flight measurement set-up.

I.C QDC-TDC MnM Signal Processing

The QDC-TDC MnM works with the CARAS daughter card. In general, for QDC performing, the CARAS daughter card is used in its 50Ω-load configuration.

QDC-TDC MnM is able to compute four different charges up to 1.5 µC.

The dynamic range of the QDC-TDC MnM inputs is the dynamic range of the CARAS daughter card, i.e. +/-1.2V. The dynamic range can be shifted by adjusting an offset in FASTER V2 – FASTER GUI software. Therefore, the maximum current measured by CARAS-50Ω is about 46 mA.

Each event detected by FASTER-QDC-TDC is timestamped with a 2ns accuracy (LSB timestamp value).

For the TOF measurement, FASTER-QDC-TDC provides a 7.8ps-accuracy time data (7.8ps is the quantification bit). Time resolution versus event amplitude is shown on the following figure. This chart is obtained with a 2V-logic signal on channel 1, and a logic signal from 6mV to 2V on channel 2. But FASTER can also be operated with analog signals.

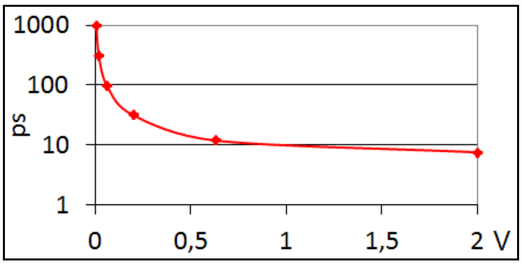

Figure 3: TOF resolution

Refer to the CARAS daughter card descriptions for more information.

II Preamble

II.A FASTER launching

To take benefit of the QDC-TDC MnM of the FASTER acquisition, the experimenter can build his experiment interface with the command `faster_setup_gui`.

The interface, shown on Figure 4, is launched. To use the FASTER QDC-TDC MnM, the experimenter must select the “QDC-TDC” type, by right-clicking on the daughterboard line.

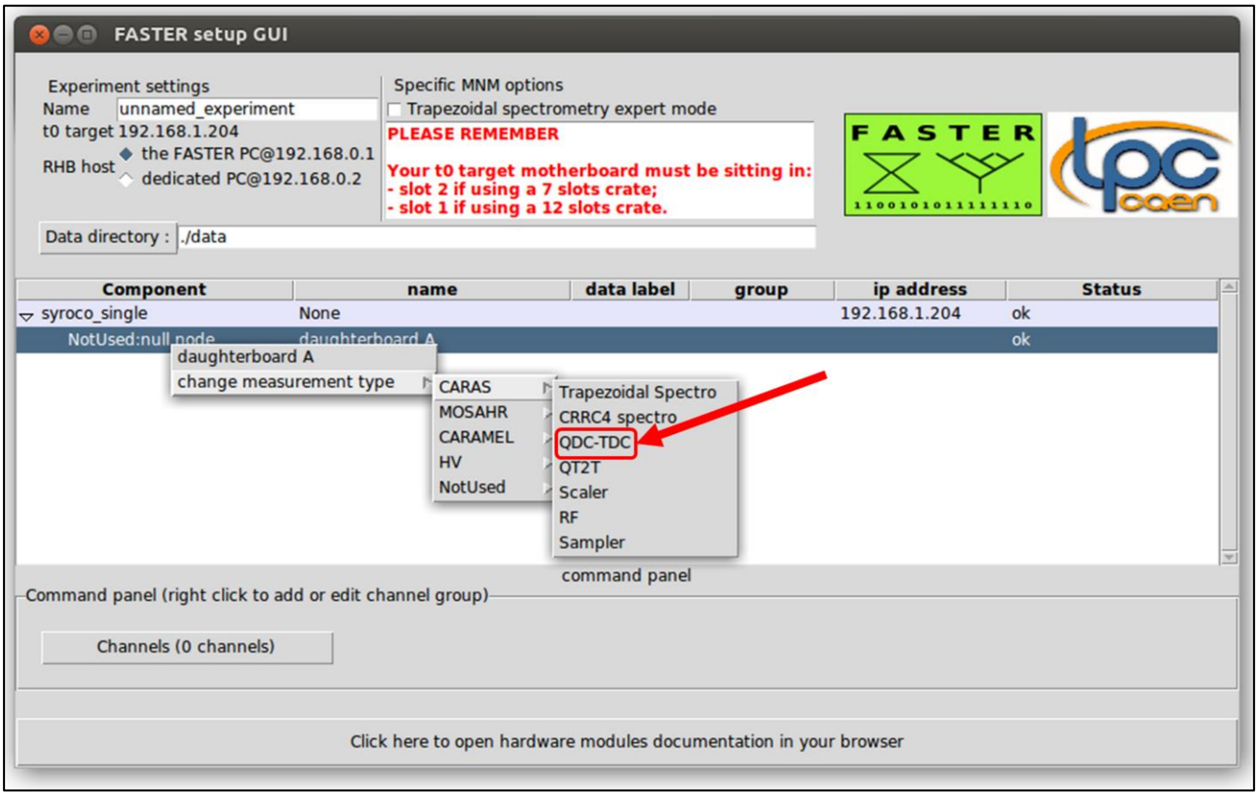

Figure 4: experiment building with "faster_setup_gui".

Before exiting the application form, the user can choose the names of the experiment, of the daughterboard and of each channel of the "daughterboard".

With the command line `faster_gui`, the experimenter accesses to the FASTER acquisition display, shown on Figure 5.

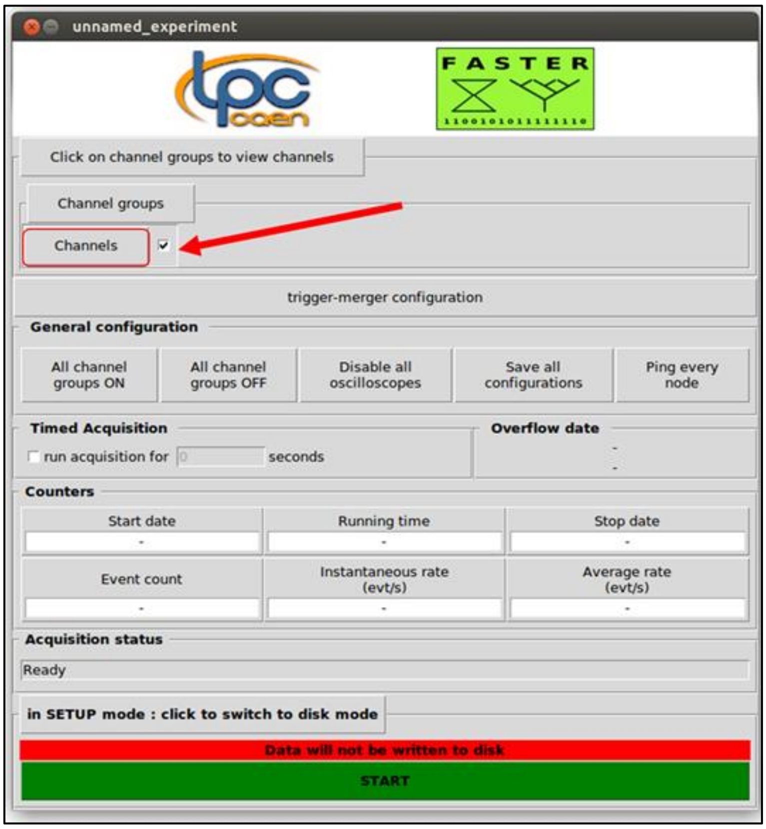

Figure 5: faster_gui interface.

By clicking on "Channels" (cf. Figure 5), the MnM interface is displayed, allowing the user to adjust the different module parameters (Figure 6).

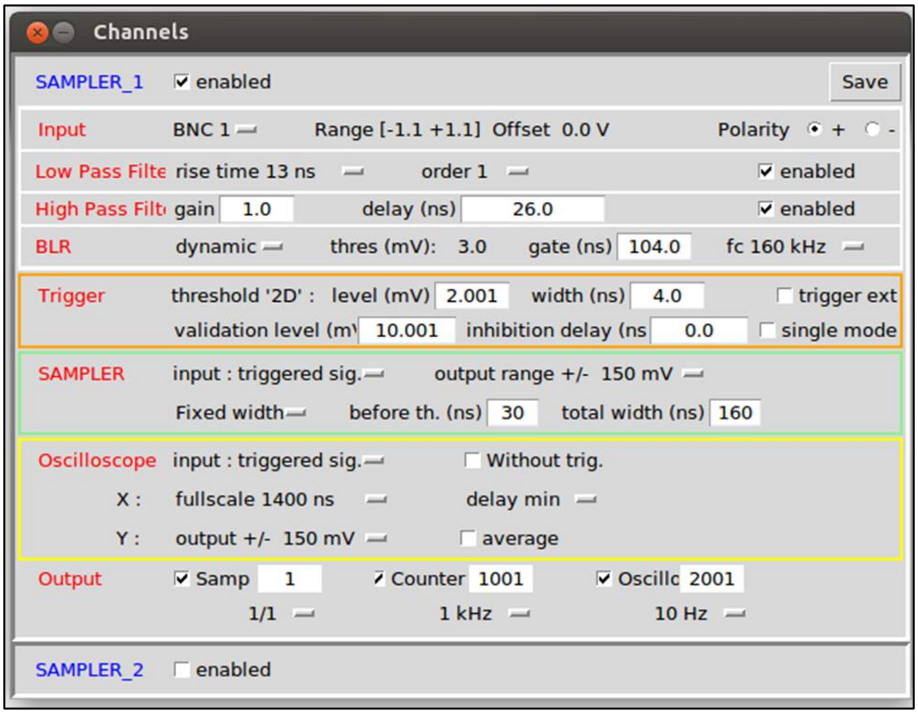

Figure 6: QDC-TDC interface

II.B RHB launching

To take benefit of RHB displays, the experimenter shall execute the command `faster_rhb_demo_qdc_copy` in the working directory, in order to have an example of RHB files adapted to the FASTER QDC-TDC MnM.

A new repertory `QDC_RHB_Demo` is created. The user shall go in the Discri repertory contained in the repertory `QDC_RHB_Demo`, before launching RHB interface.

```
cd QDC_RHB_Demo
cd Discri
RHB -r
```

III Description of QDC-TDC MnM

The QDC-TDC MnM is a signal processing module designed for signals digitalized by a 12-BIT, 500MHz analogic-to-digital converter. That means that the module receives a 12BIT-sample every 2 ns, and is able to timestamp its output data with an accuracy of 2ns (every event timestamp value has to be multiplied by 2 ns to have the event date in nanoseconds).

The QDC-TDC MnM contains the following elements:

- A dynamic range tuning,
- A polarity tuning,
- A filter if necessary,
- A baseline restorer,
- A trigger module including two kinds of discriminator,
- A charge calculation module,
- An oscilloscope,
- An event counter.

It is important to know the role of each element in order to obtain the charge spectra or the TOF spectra with the best resolution. The QDC-TDC MnM provides three kinds of 2ns-accuracy dated data:

- Oscilloscope data
- Charge module data, with an additional 7.8ps-accuracy time information in case of time measurement
- Event counter data.

This data can be displayed thanks to the Root Histogram Builder (cf. http://faster.in2p3.fr/index.php/introduction-rhb)

The QDC-TDC MnM structure of processing is shown on Figure 7 below.

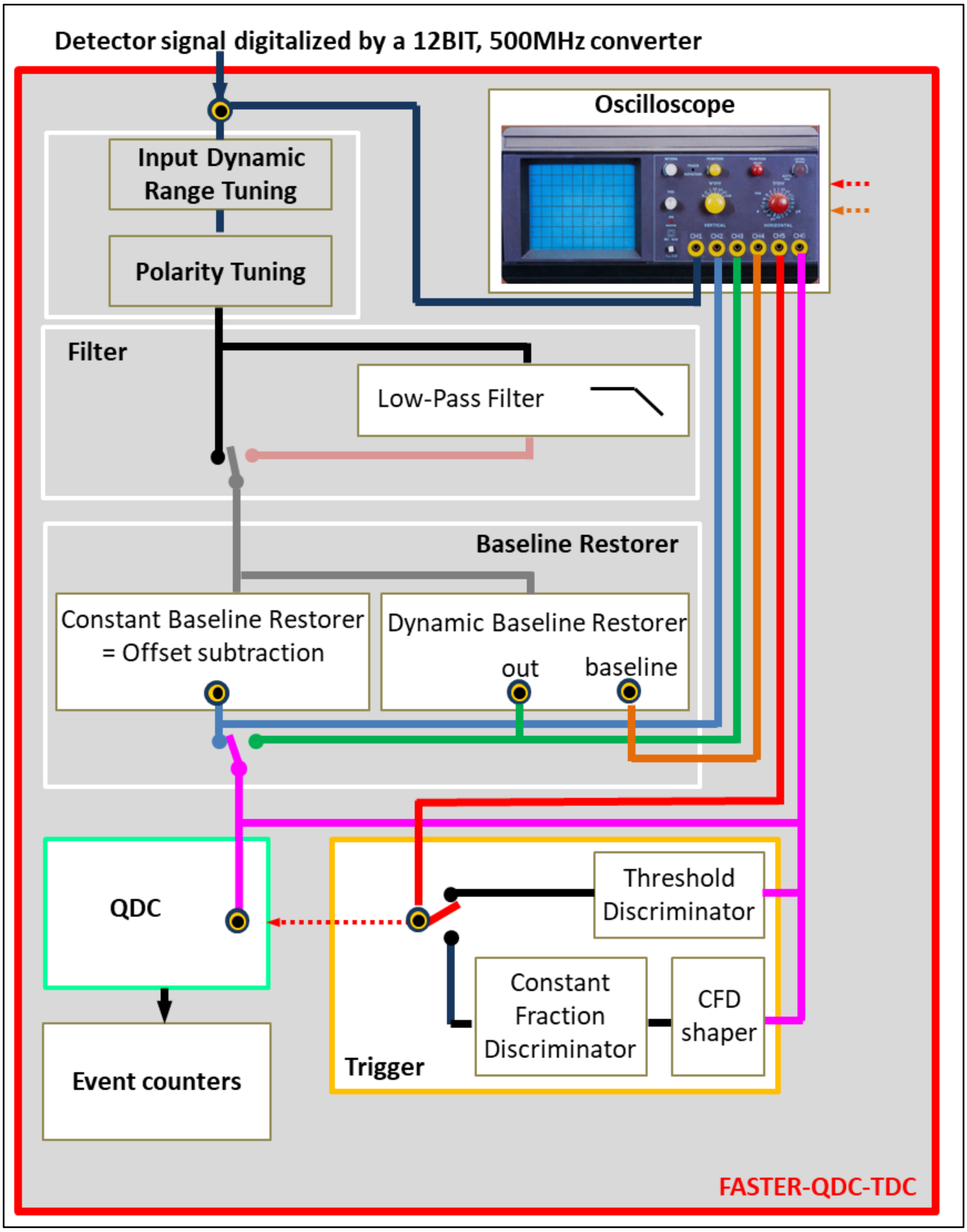

Figure 7: Diagram of the FASTER-QDC-TDC signal processing.

III.A The oscilloscope module

The oscilloscope displays the signal at the output of the various modules described later.

⚠ It is not calibrated, and the scale in millivolts of the y-axis is only an indication of the voltage.

Nevertheless, the FASTER oscilloscope includes several features found on any ordinary oscilloscope, like trigger choice, channel display choice, horizontal tuning, and vertical tuning. Additionally, the FASTER-QDC-TDC processing lets you select the acquisition speed.

III.A.1 The oscilloscope trigger choice

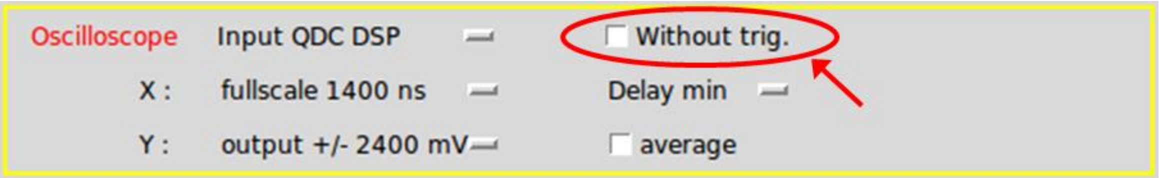

Figure 8: Trigger mode parameter

The oscilloscope display can be triggered by the discriminator module or not. During the initial settings, it's very useful to select "Without trig.". This tuning helps to identify the shape of the signal, and its polarity.

III.A.2 The oscilloscope input channel

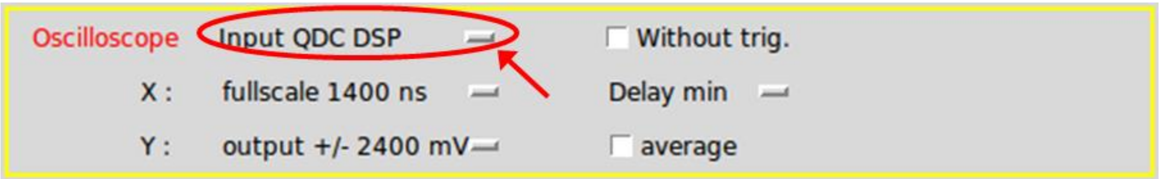

Figure 9: The inspected channels

The oscilloscope displays several signals from different modules:

- "Input Raw Signal": The FASTER daughter card includes an analogic-to-digital converter. This channel shows data digitalized by this converter.
- "Input Constant BLR": This channel shows data after the "constant baseline restorer" processing unit. Refer to sectionIII.D.1 .
- "Input Dynamic BLR": This channel shows data after the "dynamic baseline restorer" processing unit. Refer to section III.D.2 .
- "Input Dyn Base Line": This channel shows the baseline computed by the "dynamic baseline restorer" processing unit. Refer to section III.D.2 .
- "Input Trigger": This channel shows the signal used by "Trigger" module. Refer to section III.E .
- "Input QDC DSP": This channel shows the signal used by "Charge Calculation" module. Refer to section III.F .

III.A.3 The oscilloscope horizontal tuning

The time base of the signals can be adjusted with 3 parameters: shift, fullscale, subsampling.

III.A.4 The horizontal fullscale

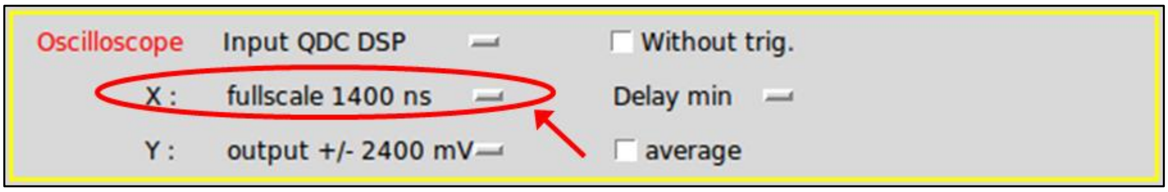

Figure 10: The horizontal fullscale parameter

The user can select between 9 fullscale ranges from 6µs to 1.4ms.

A signal graph contains 700 samples.

The time interval between two samples is: 2 ns for 1400 ns fullscale range; it is the sampling period of the 500MHz analogic-to-digital converter. The time interval is 4 ns for 2800 ns fullscale range, 8 ns for 5600 ns fullscale range, 16 ns for 11 µs fullscale range, 32 ns for 22 µs fullscale range, 64 ns for 45 µs fullscale range, 128 ns for 90 µs fullscale range, 256 ns for 180 µs fullscale range, 512 ns for 360 µs fullscale range, 1024 ns for 0.7 ms fullscale range, 2048 ns for 1.4 ms fullscale range.

III.A.5 The subsampling mode

Figure 11: The subsampling mode parameter

As the number of samples is constant, the time interval between two samples is different according to the horizontal fullscale. When this time interval is greater than 2 ns, there are two ways to subsample the signal:

- Either every sample of the oscilloscope display represents the average of several samples. It's the "average" mode.
- Or every sample of the oscilloscope display represents one sample every N samples. It's the "subsampling" mode.

⚠ When a very short signal must be displayed, don't forget to change the horizontal fullscale to 1400ns fullscale. In "average mode", the average of a very short signal within a lot of samples is almost zero. In "subsampling mode", the sample shown is not necessarily the peak sample of the short signal. Therefore, a short signal exits, but it can be not-displayed.

III.A.6 The delay

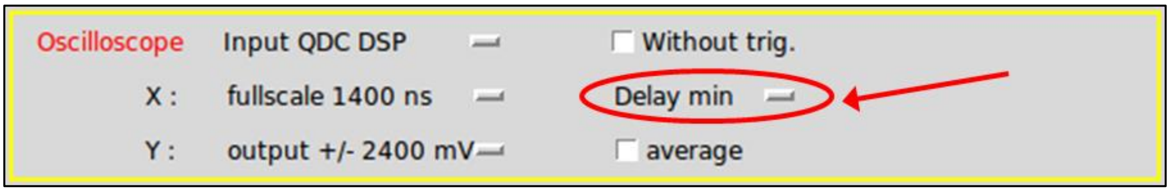

Figure 12: The delay parameter

This parameter is available only when the oscilloscope display is triggered by the discriminator module.

The sample, that satisfies discriminator module conditions, is set at the very beginning (delay min), 25%, 50% or 75% of the display.

⚠ The sample, which satisfies the discriminator module conditions, is always placed at abscissa "0 ns" on the oscilloscope display.

III.A.7 The oscilloscope vertical tuning

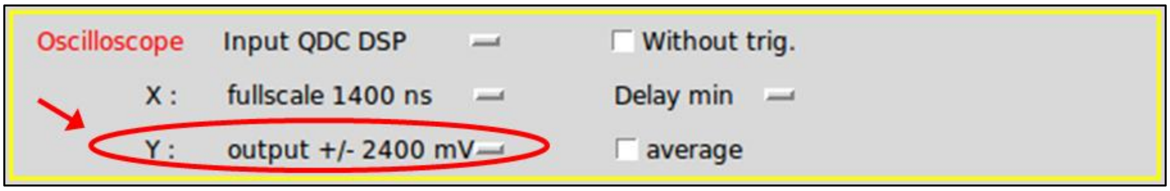

Figure 13: The **vertical fullscale**

The values of the oscilloscope samples are always signed 16 BIT values, centered on 0.

The QDC-TDC MnM is processing 12 BIT signal samples for a fullscale around 2.4V peak to peak. But, as the signal is not 0-centered, the processing module uses 13BIT for +/-2.4V fullscale.

In order to perform high-resolution calculations in the processing, 7 BIT are added as accuracy BIT on the signal sample.

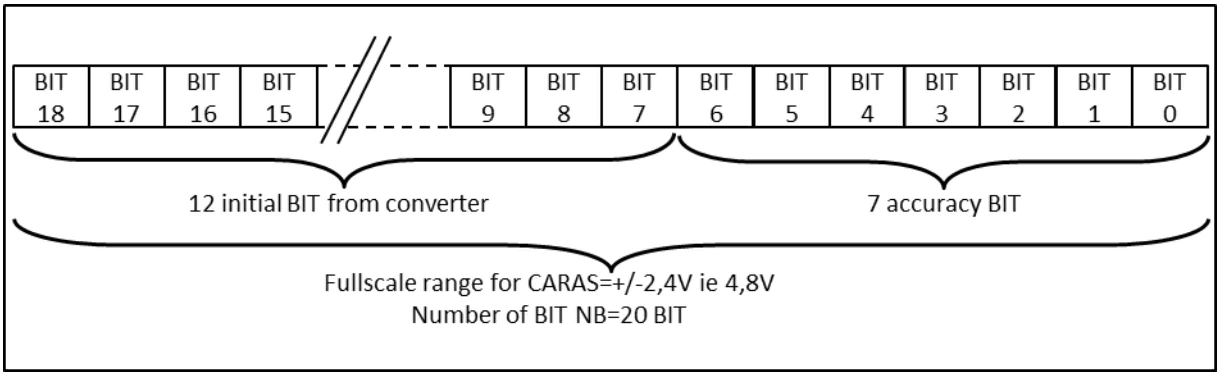

Figure 14: Data representation in the processing module

The values of the oscilloscope module have only 16 BIT. Several oscilloscope fullscale ranges are available to make the most of the maximum accuracy, or of the maximum fullscale of the QDC-TDC MnM.

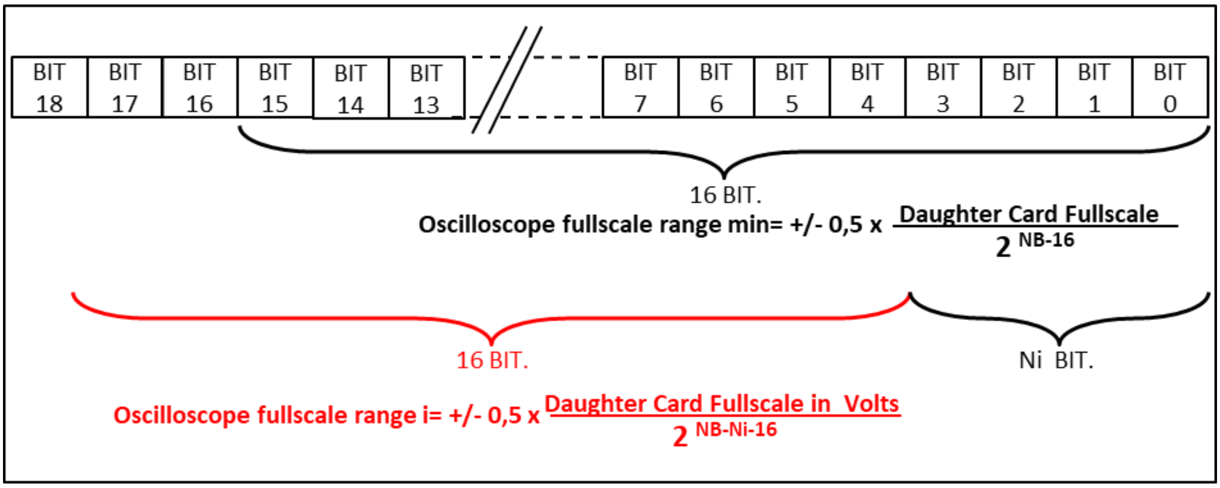

Figure 15: The oscilloscope fullscale ranges

For example:

Oscilloscope fullscale range min $= \pm\, 0.5\ \frac{4.8\text{V}}{2^{20-0-16}} = \pm 150\text{mV}.$

The oscilloscope fullscale range does not affect the internal representation of the signal used by the module.

III.A.8 The oscilloscope acquisition speed

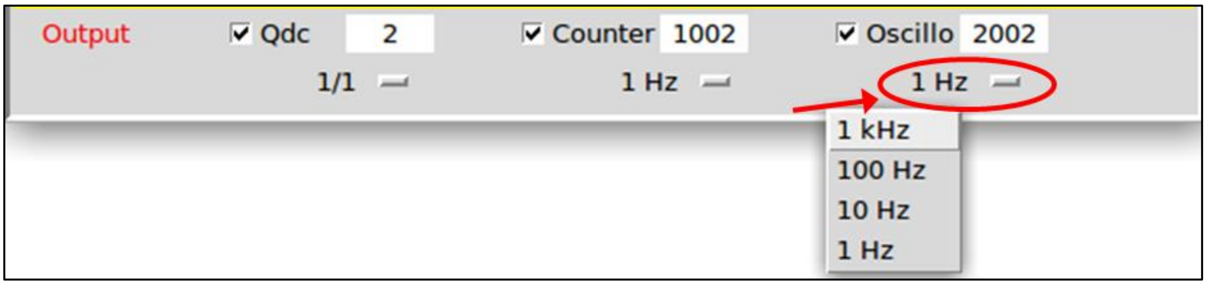

Figure 16: The acquisition speed parameter

There are 4 choices of acquisition speed:

- One acquisition every 1 millisecond: 1 kHz,
- One acquisition every 10 milliseconds: 100 Hz,
- One acquisition every 100 milliseconds: 10 Hz,
- One acquisition every second: 1 Hz.

III.A.9 The oscilloscope output data

An oscilloscope data consist of 1440 bytes. This data contains the event timestamp, the time scale, the time offset, the mV scale, and the 700 samples.

III.B The Input module

III.B.1 CARAS Data Channel Selection

CARAS daughter card has two analog input channels. They may be processed by two QDC-TDC MnMs implemented in one FPGA on the mother card. Two internal multiplexers are used to select the analog channel processed by the QDC-TDC MnMs (cf. Figure 17).

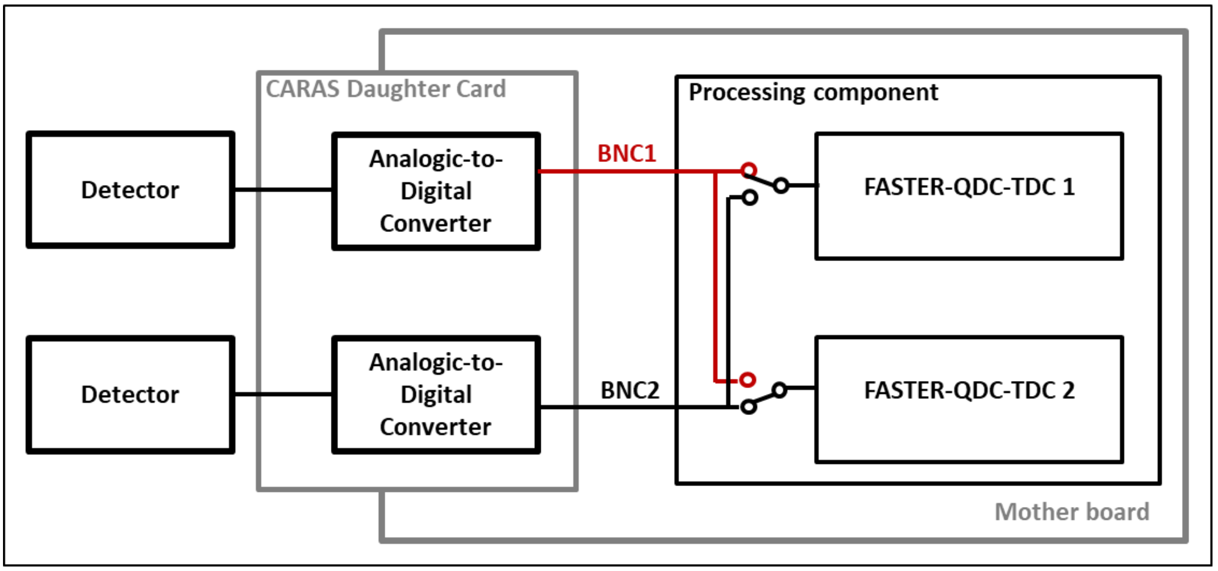

Figure 17: Multiplexers to select which analog channel to be processed.

Therefore, the first parameter to select is the "input BNC channel", as shown on Figure 18. One MnM will then be linked with one analog channel.

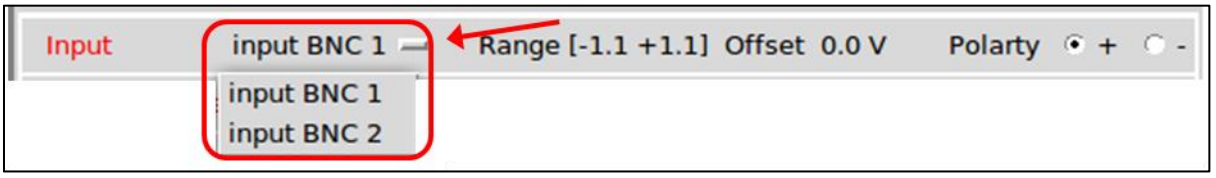

Figure 18: Analog channel selection for MnM processing.

III.B.2 The "Input Dynamic Range Tuning" module

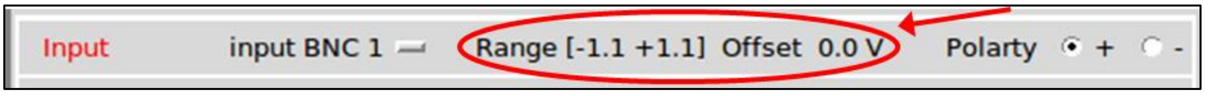

Figure 19: Input range adjustment for CARAS daughter card

The second parameter to adjust is the dynamic range. The input ranges from -1.195V to 1.195V, if you don't change anything. Only one range can be selected for an input BNC channel.

By electrically changing the offset level, you can take advantage of the full scale range of about 2.4V. You can increase or decrease the input signal baseline level from -1.1V to 1.1V.

The raw data (that means the data digitized by the converter) is viewable with the "Oscilloscope" module. It is always between -1.1V and 1.1V.

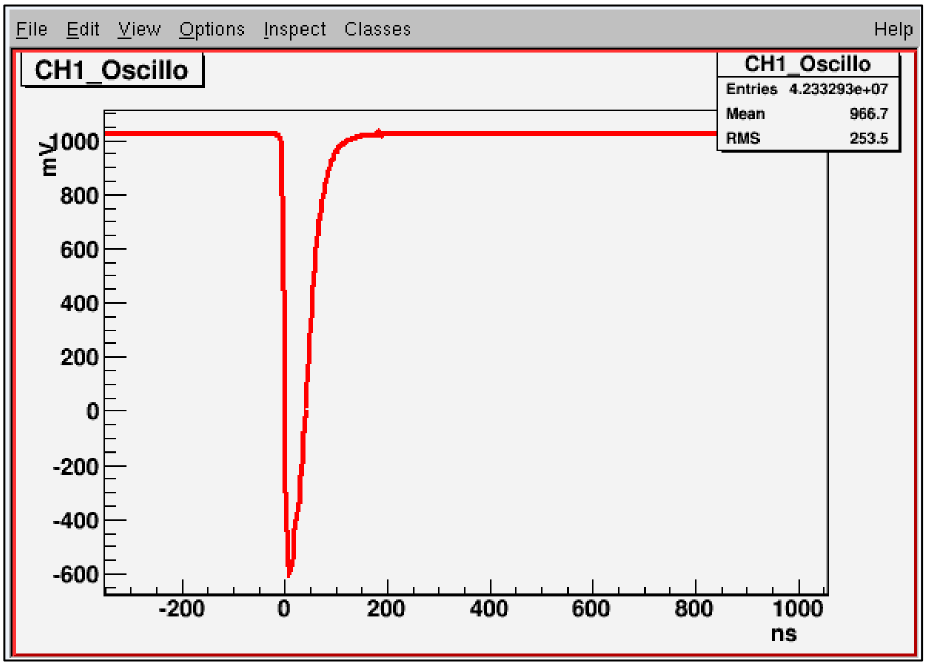

Figure 20: The data from detector can range up to 2V and stays in the CARAS dynamic range.

In this example, the input range is set to 1000mV in order to take advantage of the full 2.4V analog range.

III.B.3 The "Polarity Tuning" module

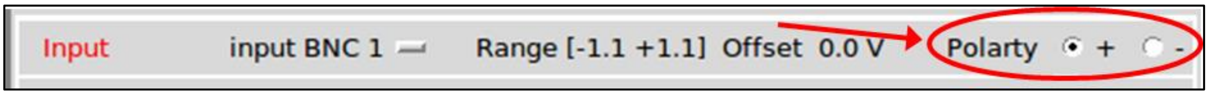

Figure 21: The polarity parameter

The FASTER-QDC-TDC process uses positive values. If the detector provides a negative signal, it is essential to convert it into a positive signal.

III.C The "Low Pass Filter" module

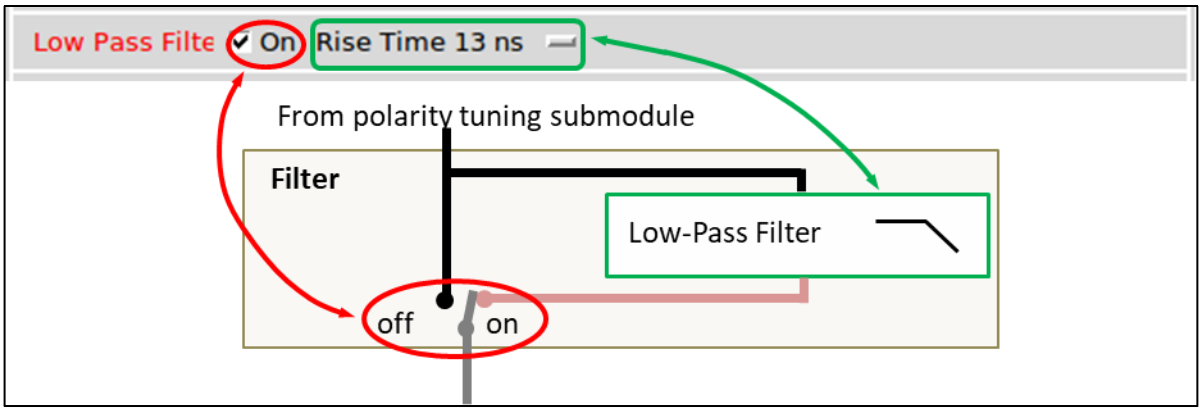

Figure 22: "Low Pass Filter" module.

If the "Low Pass Filter" module is "On" (cf. Figure 22), the signal is then low-pass filtered. The user can select one of the three available filters, defined by their rise time: either 13 ns, 27 ns or 57 ns (cf. Figure 23).

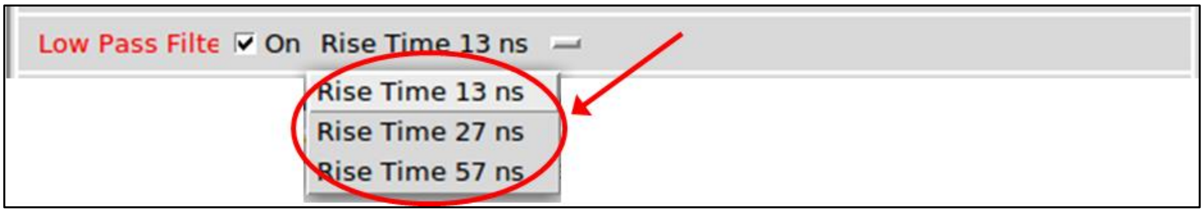

Figure 23: Low-pass filter rise time.

Using Low Pass Filters avoids triggering on pulse spikes or noise, but signal is more spread over time.

III.D The "Baseline Restorer" module

In order to obtain charge spectra or TOF spectra with the best resolution, it is necessary to zero the acquired signal baseline. The "Baseline Restorer" module provides two ways to zero the baseline:

- Either by subtracting a constant level: that is the constant BLR
- Or by subtracting a signal which follows the low input signal variations: that is the dynamic BLR.

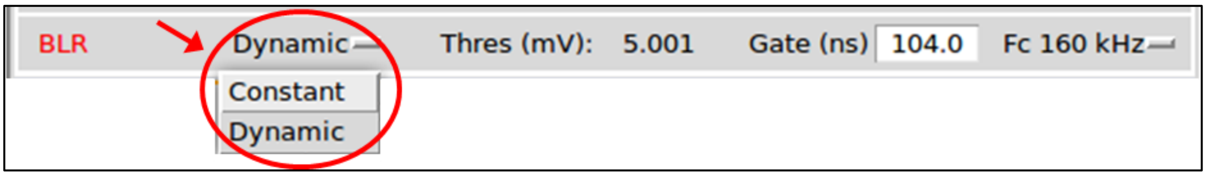

Figure 24: the BLR choice parameter.

III.D.1 The "Constant Baseline Restorer" module

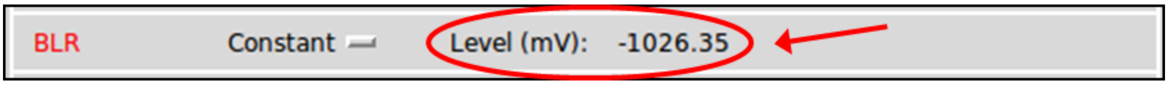

Figure 25: The "Level" parameter of the Constant BLR module

This baseline restorer simply subtracts a constant level.

III.D.2 The "Dynamic Baseline Restorer" module

This baseline restorer follows the slow variations of the signal baseline.

Figure 26: The dynamic baseline restorer parameter

Theory of operation:

The theory of operation of the baseline restorer is shown below:

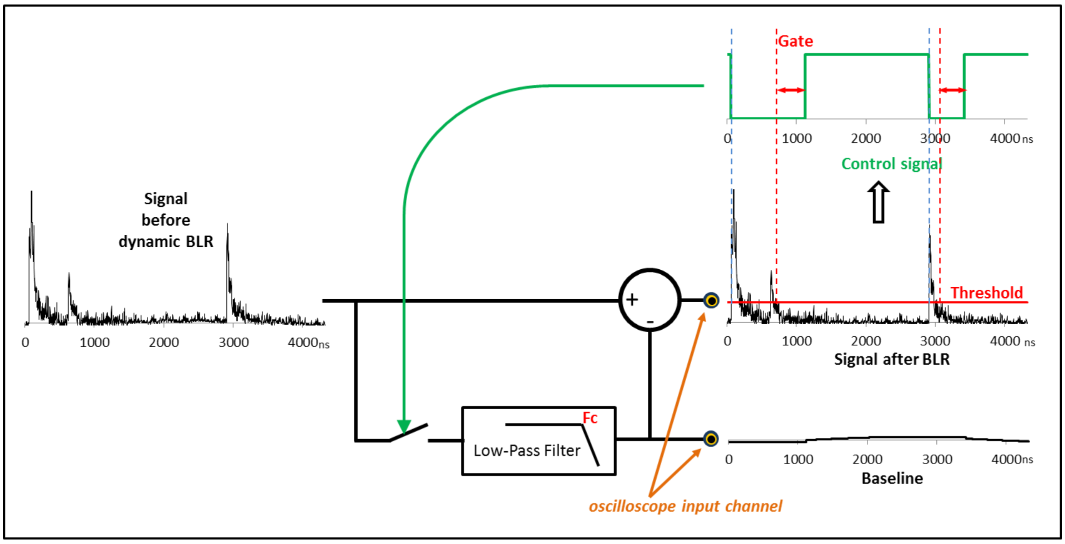

Figure 27: Theory of operation of baseline restorer: "Threshold", "Gate" and "Fc" have to be tuned.

The signal from the "Polarity Tuning" module is filtered by a low-pass filter. This tracking filter lets through any slow variations of the signal. The **cut-off frequency "Fc" of this low-pass filter** is 20 kHz, 160 kHz, 640 kHz or 6600 kHz. It is a first order low-pass filter.

The baseline tracking by the low-pass filter is stopped when an event is detected. That means when the cleaned **signal after BLR exceeds a "± threshold" parameter value**. Then the baseline tracking stops while the value of signal samples is above the threshold and after a **duration defined in the "Gate" parameter**. Thus, the signal tracking is stopped during all the signal duration. When the baseline tracking is stopped, the computed baseline value is set to the baseline value just before the detected event. In case of pile up, the computed baseline value is equal to the baseline value just before the first detected event.

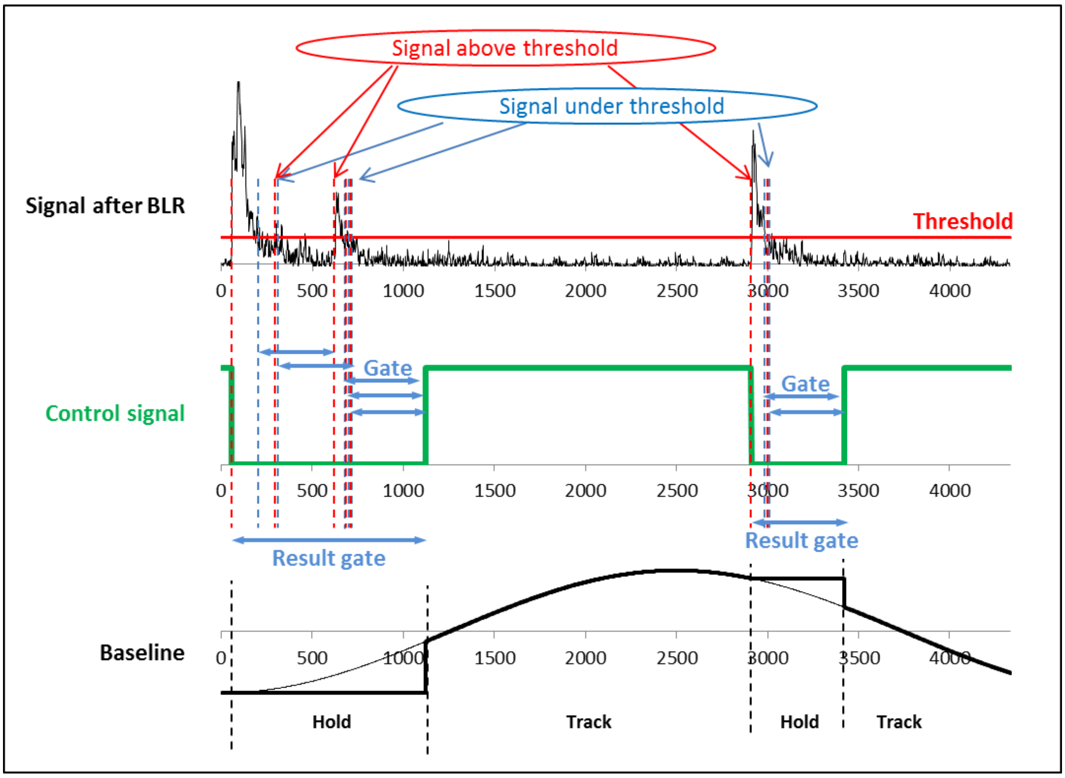

Figure 28: Focus on the BLR signal

⚠ It is important to properly adjust the automatic baseline restorer: that means adjust the threshold (“Thr(mV)”), the cut-off frequency (“Fc”), and the duration (“Gate”).

⚠ It is necessary that the “Dynamic BLR” module spends enough time to compute the baseline. If the event flow rate is too high, the low-pass filter is no longer able to track enough the signal baseline. It is better to use “constant BLR”.

⚠ The “Dynamic BLR” module can’t be in its hold state during more than 400 µs. After 400µs, whatever the signal, it will be considered as a baseline.

Dynamic baseline restorer adjustment:

The BLR Threshold:

When tuning the BLR threshold, you must inspect the “Input Dynamic BLR” signal with the internal oscilloscope. Threshold level should be chosen just above noise. The danger of setting the BLR threshold too high is that an event may be considered as a baseline, and the dynamic baseline restorer is incorrectly adjusted.

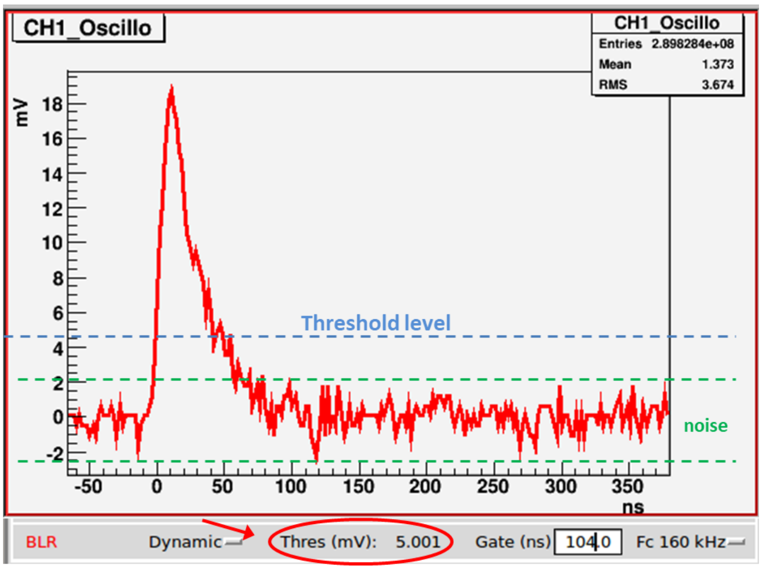

Figure 29: Baseline restorer threshold tuning

The BLR gate:

When tuning the "Gate" parameter, you must still inspect the "Input Dynamic BLR" signal with the internal oscilloscope. You have to fill in "Gate" with duration from the time when the signal passes below the threshold until signal is no more considered as an event. The maximum gate is 32760ns.

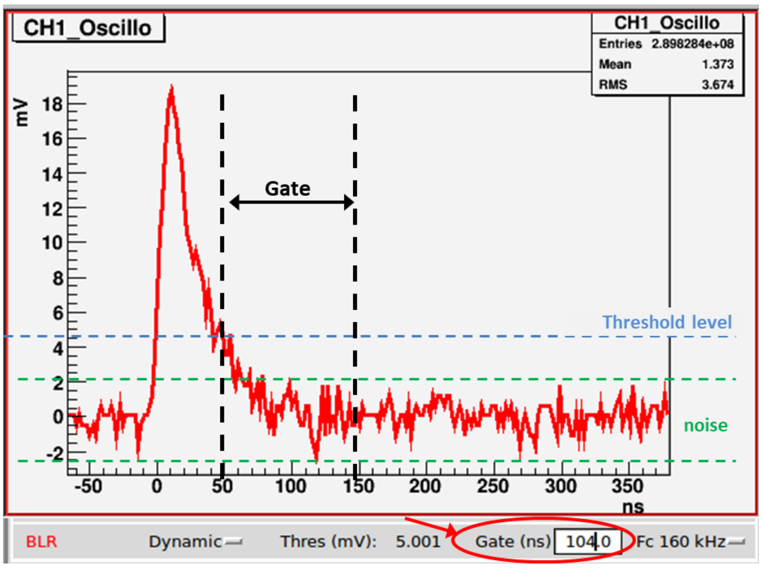

Figure 30: The BLR Gate parameter

If you have difficulties to define the gate width, fill in the parameter with the pulse duration, especially if the data flow is low.

The BLR cut-off frequency:

The "Fc" parameter is the cut-off frequency of the BLR low-pass filter. The higher this frequency, the faster the baseline is followed by the BLR module: with a 20 kHz cut-off frequency, the BLR filter tracks the baseline in 17.6 µs. It is 2.2 µs for Fc=160 kHz, 550ns for Fc=640 kHz and

53 ns for Fc=6600 kHz. Nevertheless the lower the frequency, the better the signal to noise ratio. The choice depends on the event flow, and the EMC shielding.

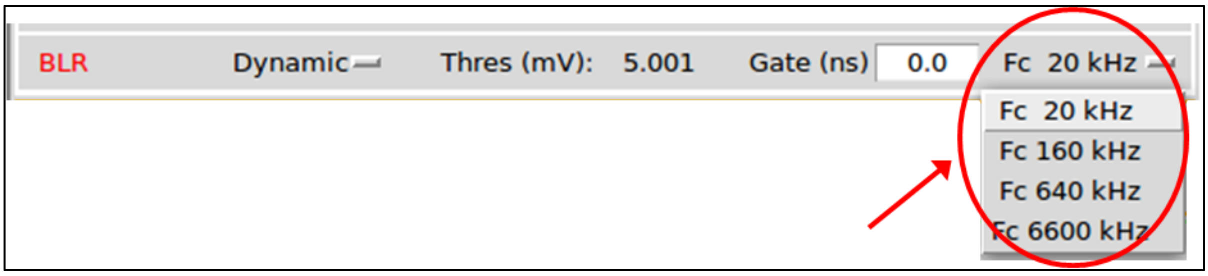

Figure 31: The BLR Cut-off frequency parameter

- *160 kHz is often a good compromise!*

⚠ When adjusting "gate" width, you can sometimes see the effect of the "Dynamic BLR" and its cut-off frequency. That happens with signals that have very long decay constant. On the following left chart (Figure 32), the "gate" width is set to 0. The "dynamic BLR" module tracks signal while samples are under the threshold. On the right chart (Figure 32), the "gate" width is wide enough to contain all of the pulse.

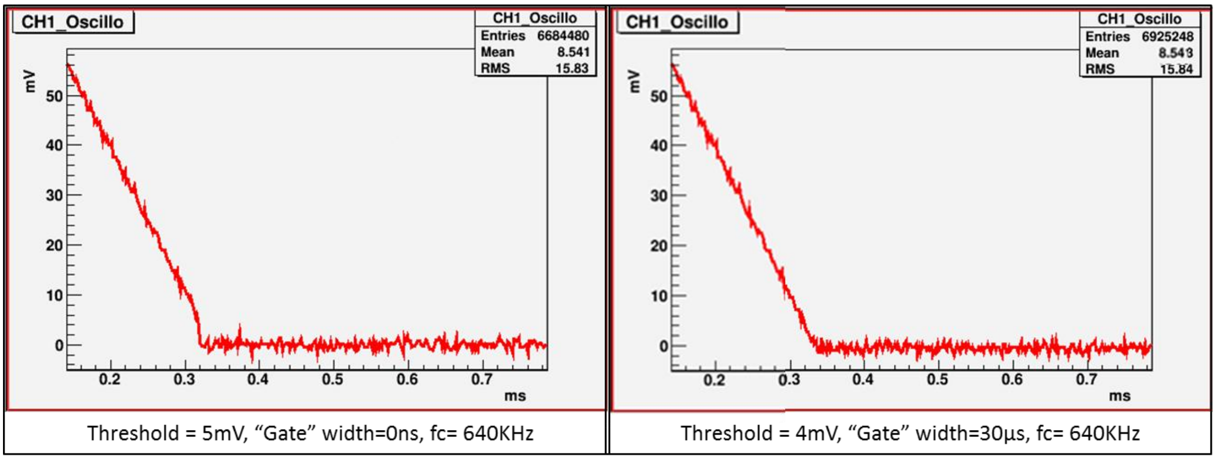

Figure 32: The "Gate" width adjustment

⚠ The dynamic BLR significantly improves the spectra resolution. But if the baseline restorer is incorrectly adjusted, the resulting charge spectra could be disastrous. You should then use the constant BLR.

III.E The "Trigger" module

The "Trigger module" mainly includes a threshold discriminator and a constant fraction discriminator (CFD). Nevertheless the FASTER-QDC-TDC processing can use an external trigger. When an event is detected by the trigger module, this event is timestamped with a 2ns accuracy clock. A 7.8ps accuracy information is added when using the CFD.

III.E.1 Internal or External Trigger

There are two QDC-TDC MnMs implemented in one FPGA on the mother card. Each MnM has an internal trigger, but a MnM can use the trigger of the adjacent MnM (cf. Figure 33) by selecting "Type EXT" (Figure 34).

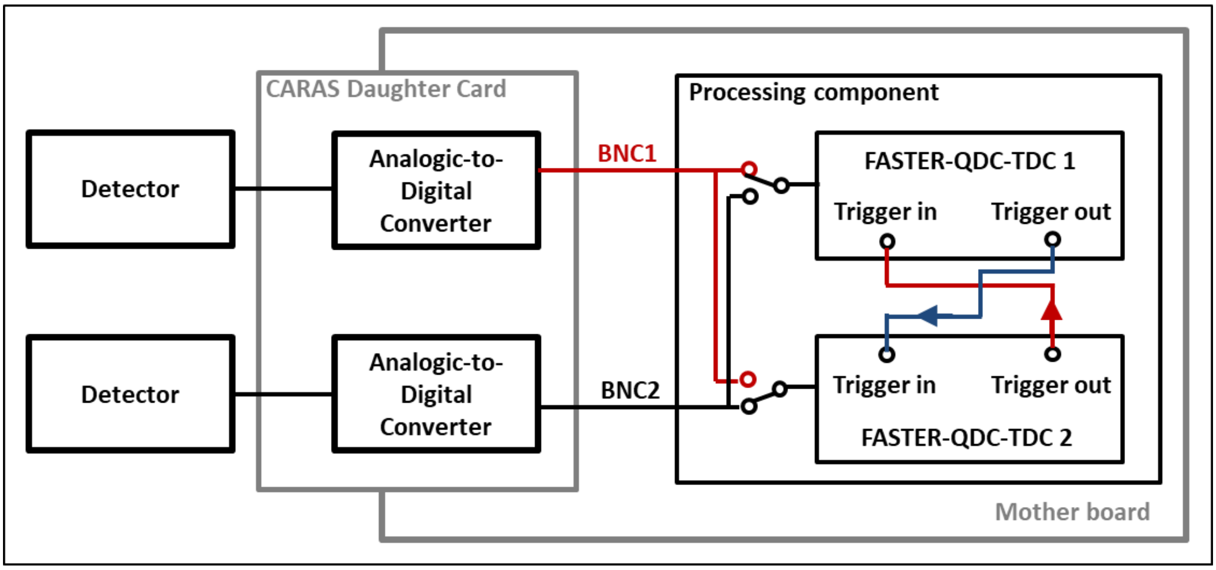

Figure 33: Crossed trigger diagram.

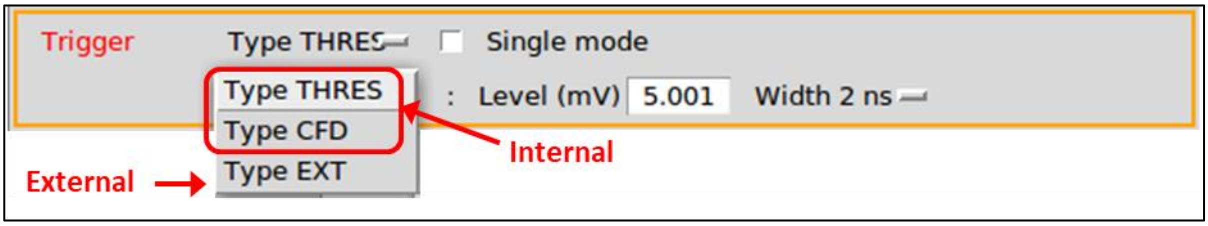

Figure 34: The internal or external trigger.

III.E.2 The parameters of the internal trigger

The internal trigger module includes the main elements shown Figure 35. Each element is going to be described.

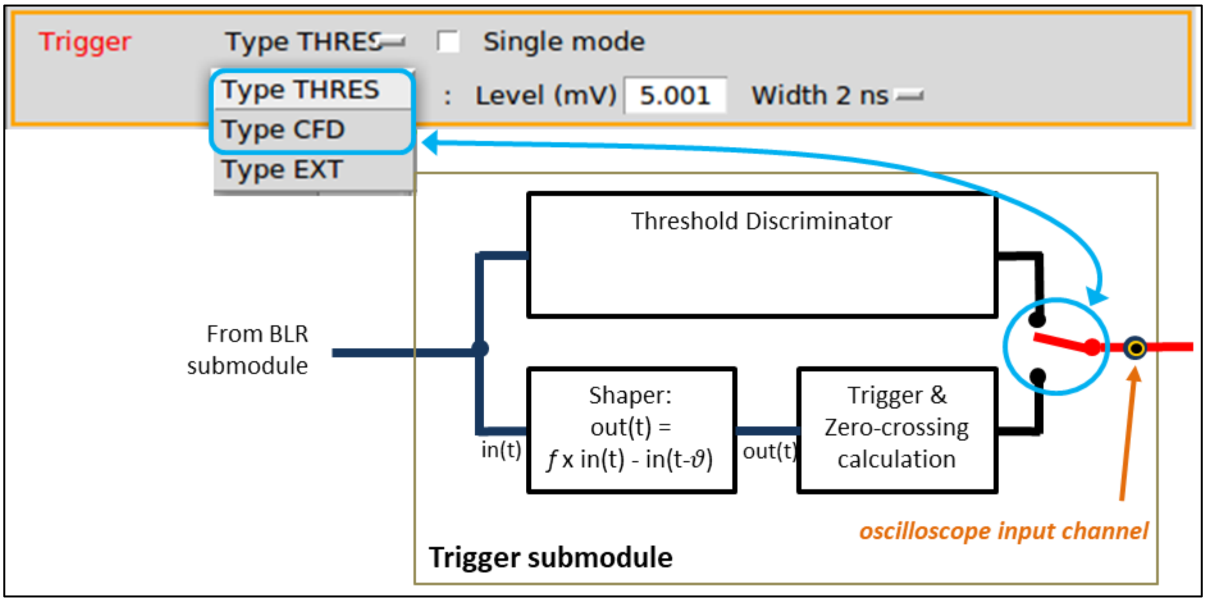

Figure 35: The internal Trigger

III.E.2.a The single mode

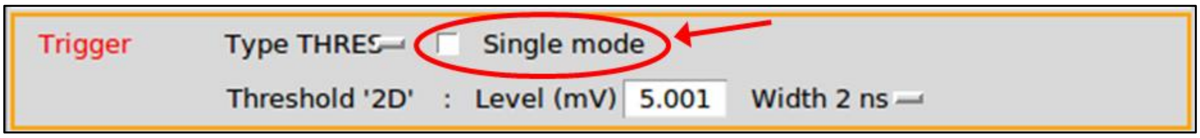

Figure 36: The "Single mode" parameter.

It is sometimes convenient to trigger in "single mode" (Figure 36) while performing the setup operation. That means that, after the first trigger found, the "trigger" module is disabled. The just-emerged sample on the charge spectrum and the oscilloscope graph represent the same event. The "Trigger" module can be reactivated by clicking on "Arm" button (Figure 37).

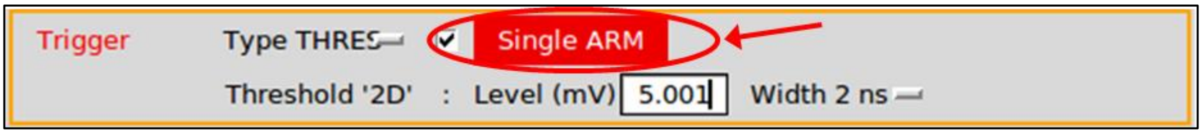

Figure 37: the "Single Arm" button.

⚠ After setup operation performing, don't forget to uncheck "Single Mode".

III.E.2.b The threshold discriminator

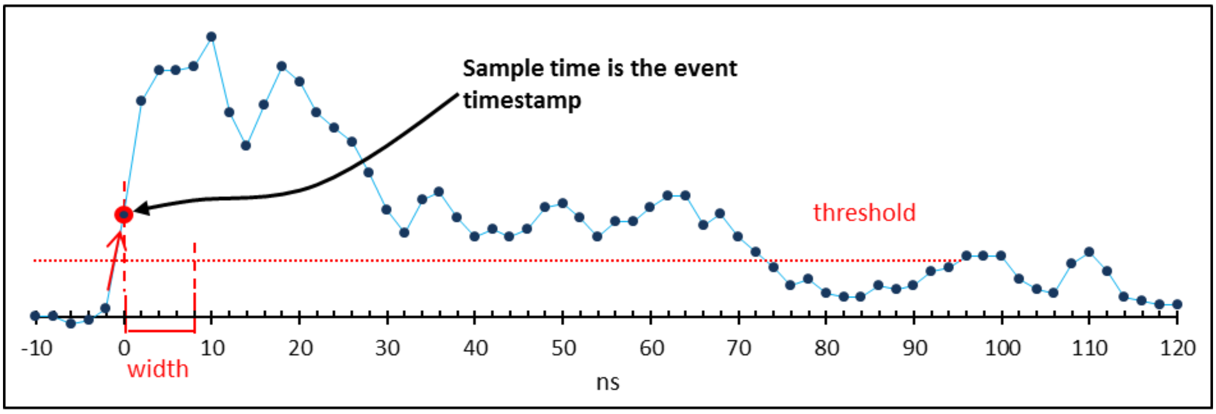

Figure 38: The threshold trigger conditions

Three conditions are required for the module to send a trigger signal:

- The signal sample is above the threshold defined by the user:

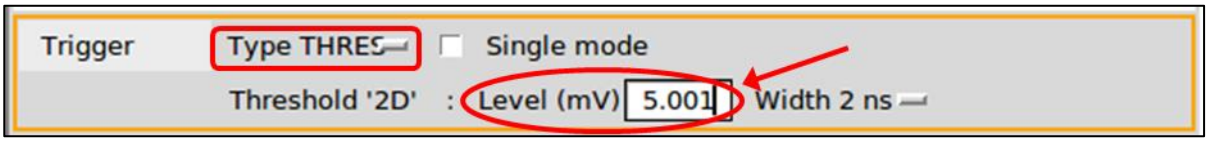

Figure 39: Threshold level parameter

- The triggering occurs on a rising edge
- The samples are above the threshold during a time window, which has a width defined in the "width" parameter:

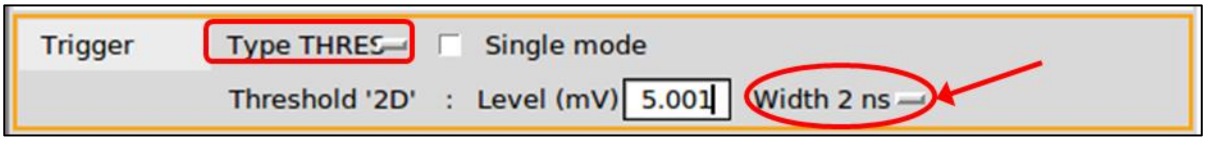

Figure 40: Time window width parameter

There are eight choices of time window width: 2 ns, 4 ns, 8 ns, 12 ns, 16 ns, 20 ns, 24 ns and 28 ns. When the 2 ns width is selected, all pulses exceeding the threshold on a rising edge are triggered, because the analogic-to-digital step is 2 ns. Selecting a time width above 2 ns avoids triggering on pulse spikes or noise.

⚠ The event is timestamped with the sample time just after the trigger conditions occur. On the oscilloscope display, in "X fullscale 1400ns" configuration, this trigger time is locally set to 0 ns, instead of the timestamp value.

⚠ **The threshold discriminator is reactivated after a time equaled to max(signal width,8ns).**

III.E.2.c The Constant Fraction Discriminator

The Constant fraction discriminator (CFD) has to be used for precise TOF measurements. This method avoids the walk due to different signal amplitudes, provided the signals from the detector are homothetic.

Theory of operation:

The input signal in(t) of the CFD module is first shaped by a module that performs the following operation:

out(t) = ***f*** x in(t) –in(t-***ϑ***).

f is the fraction and ***ϑ*** is the delay.

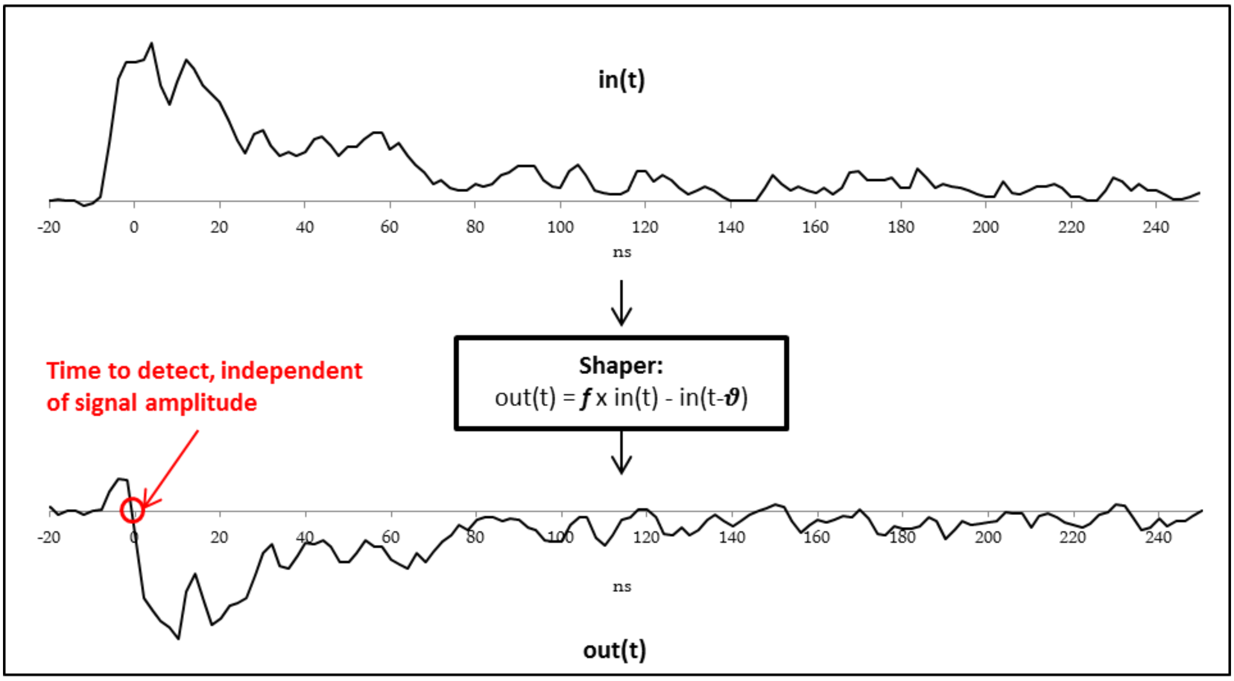

Figure 41: The CFD theory.

The module detects then the zero-crossing time. This time is independent of the in(t) amplitude. It is evaluated by a polynomial interpolation of second order.

The CFD shaper

The shaping operation is: out(t) = ***f*** x in(t) –in(t-***ϑ***).

"***f***" is the fraction and "***ϑ***" is the delay. These two parameters have to be adjusted:

- the fraction ***f*** can be set to 1/2, 1/4 or 1/8.
- the delay ***ϑ*** can be set to 2 ns, 4 ns, 6 ns, 8 ns, 10 ns, 12 ns, 14 ns or 16 ns.

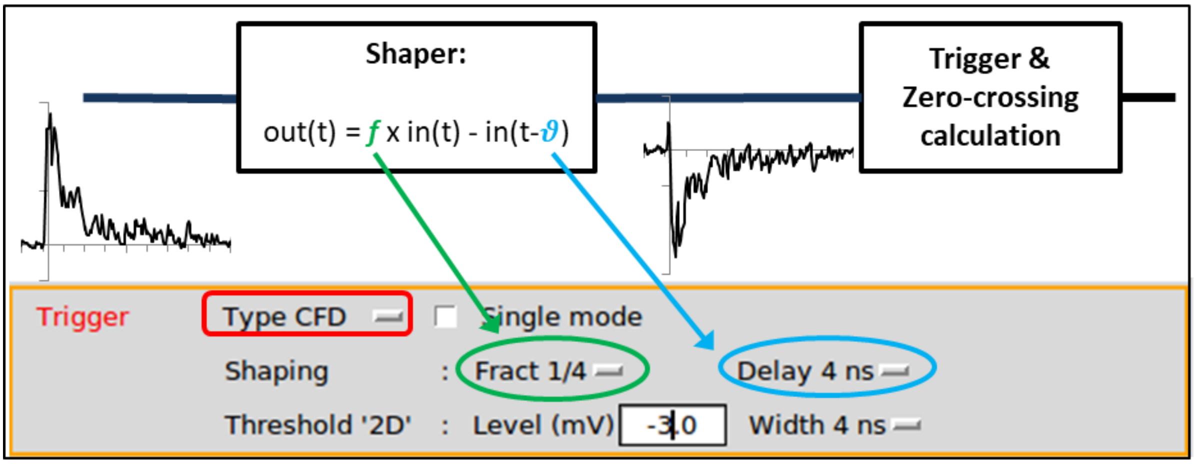

Figure 42: the fraction and delay parameters.

The constant fraction discriminator

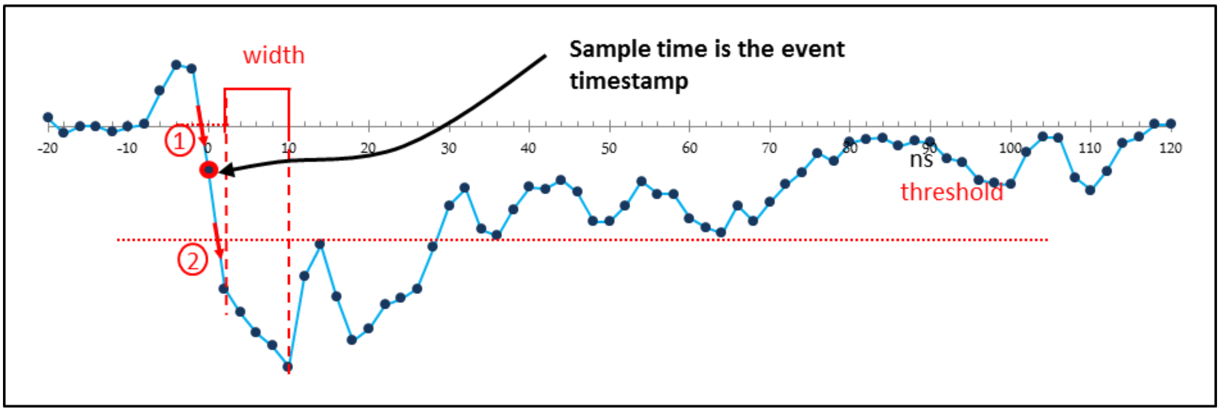

Figure 43: The CFD conditions.

Several conditions are required for the module to send a trigger signal:

- A zero-crossing on falling edge is first detected
- A threshold-crossing on falling edge is then detected, less than 24ns after the zero-crossing detection. This threshold must be negative.

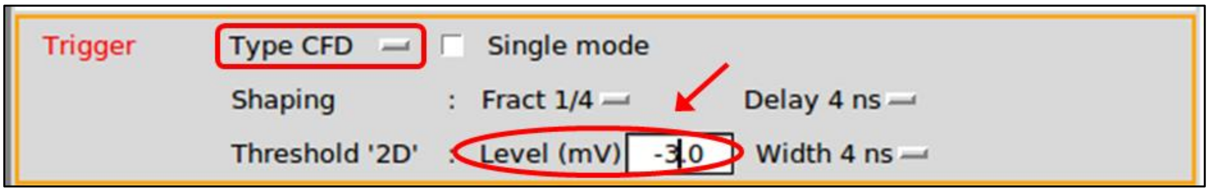

Figure 44: CFD threshold level parameter

- The samples after the threshold-crossing are under this threshold during a time window, which has a width defined in the "width" parameter:

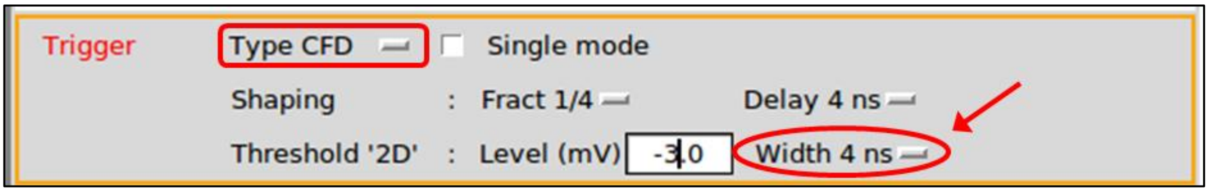

Figure 45: Time window width parameter

There are eight choices of time window width: 2 ns, 4 ns, 8 ns, 12 ns, 16 ns, 20 ns, 24 ns and 28 ns. Selecting a time width above 2 ns avoids triggering on pulse spikes or noise.

⚠ The event is timestamped with the sample time just after the trigger conditions occur. On all oscilloscope displays, in "X fullscale 1400ns" configuration, this trigger time is locally set to 0 ns, instead of the timestamp value.

⚠ **The CFD is reactivated after a time equal to max (CFD shaped signal width, 8ns).**

Time Precision calculation

The timestamp has a 2 ns accuracy. But generally, the zero-crossing – which is the true time of the event-, occurs before the timestamp date. That is why the "Trigger" module provides an additional time precision with a 7.8 ps accuracy (LSB value). This time correction is always negative range from -2 ns to 0 ns.

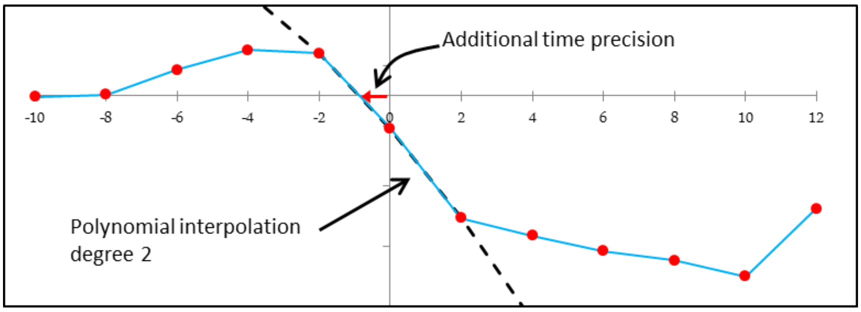

Figure 46: Time precision calculation

The polynomial interpolation uses one sample above 0 mV, and the following two samples under 0 mV.

⚠ You should be careful to the signal rise time, and the used samples for the interpolation. For example, the following chart shows that if the rise time is too high, there are not enough samples to perform a good interpolation.

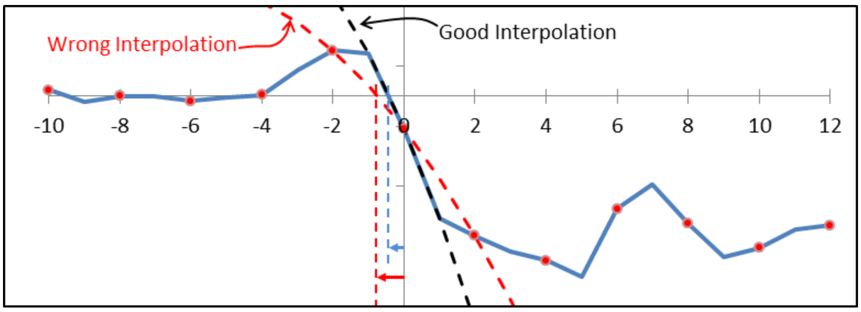

Figure 47: If the rise time is too high, the interpolation is wrong!

III.F The QDC module

The QDC module is able to compute up to four charges. The calculation consists of the integration of the input signal during a time gate defined by the user.

$$\text{CHARGE} = \sum_{t=gate\ start}^{t=gate\ end} sample(t)$$

A flag also indicates if input signal used to calculate charge is saturated.

III.F.1 Integration time gate

For each charge, two parameters need to be specified: the beginning and the end of the integration gate. In fact, the gate calculation doesn't necessarily begin when the trigger occurs. It can begin from 30 ns before the trigger occurs, up to 32734 ns after, with a 2 ns step.

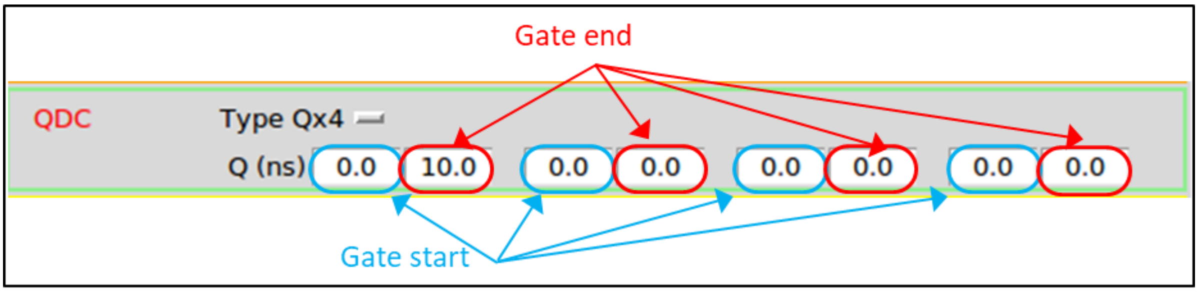

Figure 48: The time gate parameters.

III.F.2 The charge number selection

Four charges can be calculated and sent to the computer (Type Qx4), but if the experiment doesn't need as many charges, the charge number could be decreased. It could be convenient to prevent from saturation of the communication.

- -"Type Qx4" is selected when using four charges,
- -"Type Qx3" is selected when using three charges,
- -"Type Qx2" is selected when using two charges,
- -"Type Qx1" is selected when using one charge,
- "Type Tref" is selected when no charge is useful. In that case, only the event timestamp is sent to the computer. This timestamp may be supplemented by the CFD time precision.

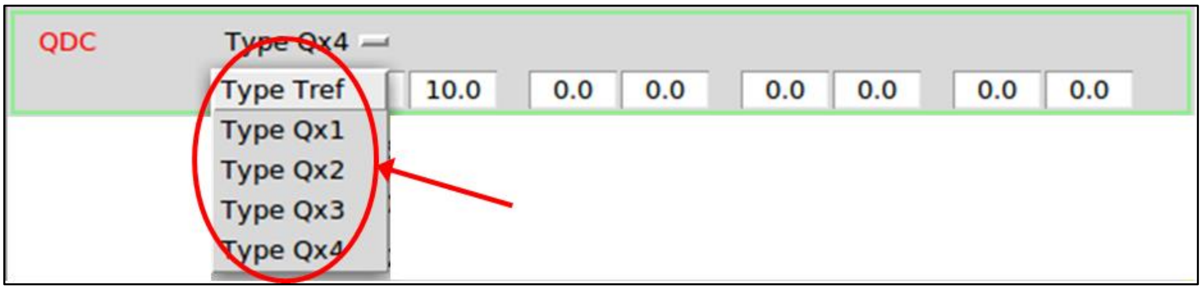

Figure 49: Charge Number selection

⚠ It is recommended to have at least one charge whose gate end includes all of the event pulse. In fact, the "Trigger" module alerts every time trigger conditions occur, even if the event pulse is not finished.

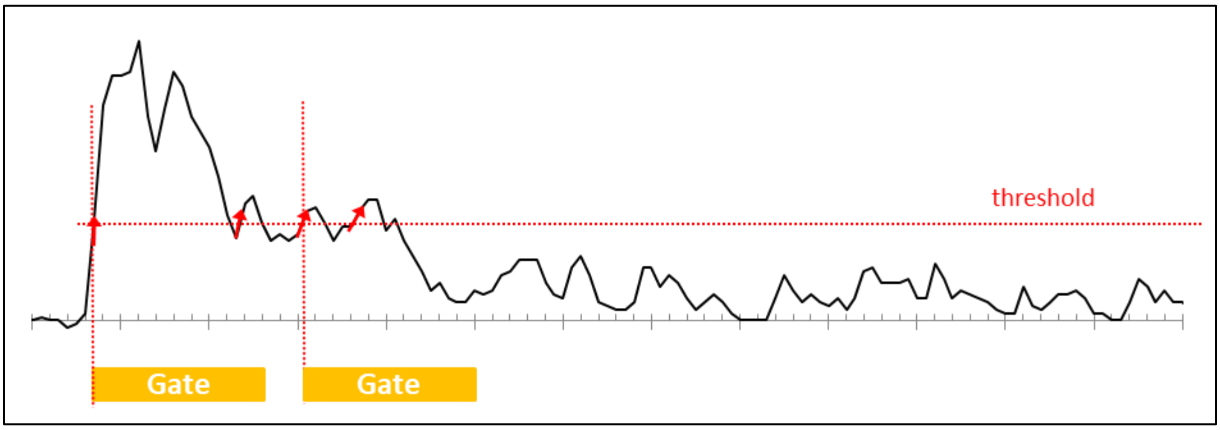

Figure 50: Example of gate too small

On Figure 50, the trigger conditions occur four times during the event pulse. The calculation gate is too small. FASTER-QDC-TDC MnM will send two charges as if there were two event pulses. Figure 51 shows a correct example of single gate (Qx1).

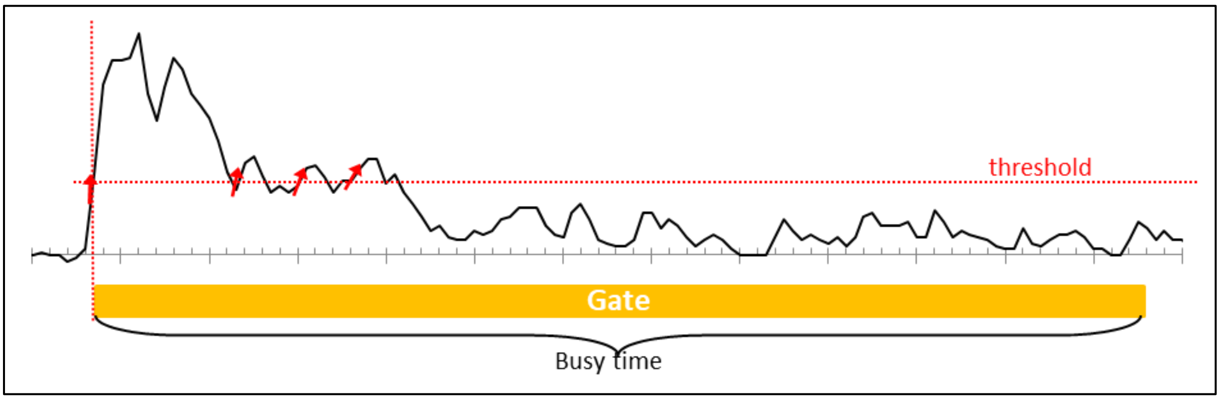

Figure 51: Example of correct single gate

III.G Data output module

The Data output module (Figure 52) defines the output data sent to the computer by checking buttons ①. These data are:

- the data processed by the QDC module ③,
- the counting data ④,
- the data from the Oscilloscope module ⑤.

To distinguish these data in the stored file, they have different labels ②. The user can moreover control the rate of output data (⑥⑦⑧).

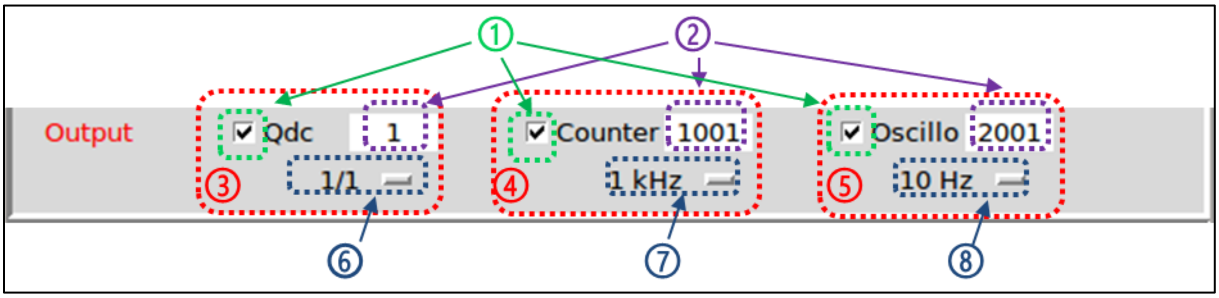

Figure 52: parameters of the Data output module

When the data comes out the FASTER-QDC-TDC MnM, they are temporally stored in some buffers of the FPGA, waiting for being sent to the computer by the Gigabit Ethernet communication.

Here are described the content of each data. If the experimenter uses RHB facilities, he has to use a the RHB file "*.pid", in which the prefix label of each channel of the FASTER acquisition is defined. The data from FASTER-QDC-TDC MnM are called,

- QDCn, if n=1 to n=4 charges are selected (Figure 49). For example, if the user selects "type Qx1", there is

  `1: QDC1: myChannel1`

- TREF, if no charge are selected (Figure 49) :

  `2: TREF: myChannel2`

That means that, in the configuration file of RHB (i.e. "*.facqConf" file):

- all data from the first channel of FASTER acquisition must have the prefix "`myChannel1_`",
- and all data from the second channel must have the prefix "`myChannel2_`".

The "`RHB -r`" command, made in the directory including these files, starts RHB interface.

III.G.1 "QDC-TDC" data

The experimenter can store or display all "QDC-TDC" data processed by the QDC-TDC module by selecting 1/1 (cf. Figure 53). But, when the event rate is too high and saturates the FASTER acquisition, the user can choose to store a percentage of this rate: one event data every 100 event data is sent, or every 10^4 event data, or one event data every 10^5 event data. With this decimation, the acquisition efficiency can be controlled.

Figure 53: Charge data decimation parameter.

In case of at least one charge used, the experimenter has, as output data:

- **myChannel_QDC1, myChannel_QDC2, myChannel_QDC3, myChannel_QDC4**: respectively charges 1, 2, 3 and 4. myChannel_QDCn is a 31-bit signed integer.

- **myChannel_QDC1_saturated, myChannel_QDC2_saturated, myChannel_QDC3_saturated, myChannel_QDC4_saturated**: the saturation flag of charge 1, 2, 3 and 4. The value 1 informs that the raw signal, that has generated the signal, when charge is calculated, is outside the input range of the daughter card.
- **myChannel_t**: the time-stamp in nanosecond of the event, with an 2 ns accuracy.
- **myChannel_dt**: an additional accuracy of the time-stamp, to achieve an accuracy of 2 ns/2^8.

In case of no charge used, the experimenter has, as output data:

- **myChannel_TREF_t**: the time-stamp (in nanosecond) of the event, with a 2 ns accuracy.
- **myChannel_TREF_dt**: an additional accuracy (in nanosecond) of the time-stamp, to achieve an accuracy of 2 ns/2^8.

III.G.2 "Counters" data

The experimenter can store and display the counting data, called "Counters" with a selected frequency of 1 Hz, 10 Hz 100 Hz and 1 kHz.

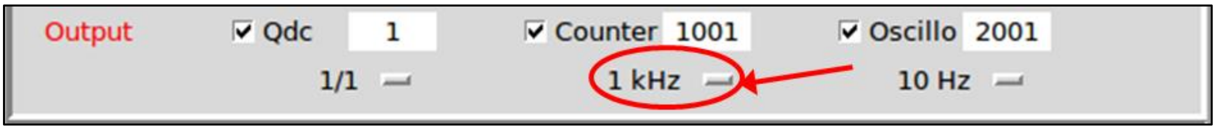

Figure 54:: The counters acquisition speed parameter

Each "Counters" data has:

- **myChannel_COUNT_t:** the time-stamp of the "Counters" data
- **myChannel_CALC**: the number of events that the QDC module has processed.
- **myChannel_SENT**: the number of data from QDC module, temporally stored in the FPGA buffers, and waiting for being sent to the computer.

The following inequality is always verified: myChannel_SENT≤ myChannel_CALC.

These 2 numbers are reset each time any module parameters is changing.

III.G.3 "Oscillo" data

The "Oscillo" data, already explained in chapter III.A , are defined in RHB by the variables:

- **myChannel_OSC_t**: the time stamp of the "0 ns" sample of the oscilloscope frame.
- **myChannel_OSC**: the Oscilloscope frame.

III.H Dead time

III.H.1 Dead time of the "QDC" data

As shown on Figure 55, the dead time of the event processed by the QDC-TDC module depends on:

- the pulse width W_{tt}, i.e. the duration between the moment when the incoming signal of the "trigger" module crosses the "trigger" threshold on rising edge and the moment when this signal crosses the same threshold on falling edge.
- The maximum gate duration D_g, i.e. the difference between the higher gate boundary and the lower gate boundary.

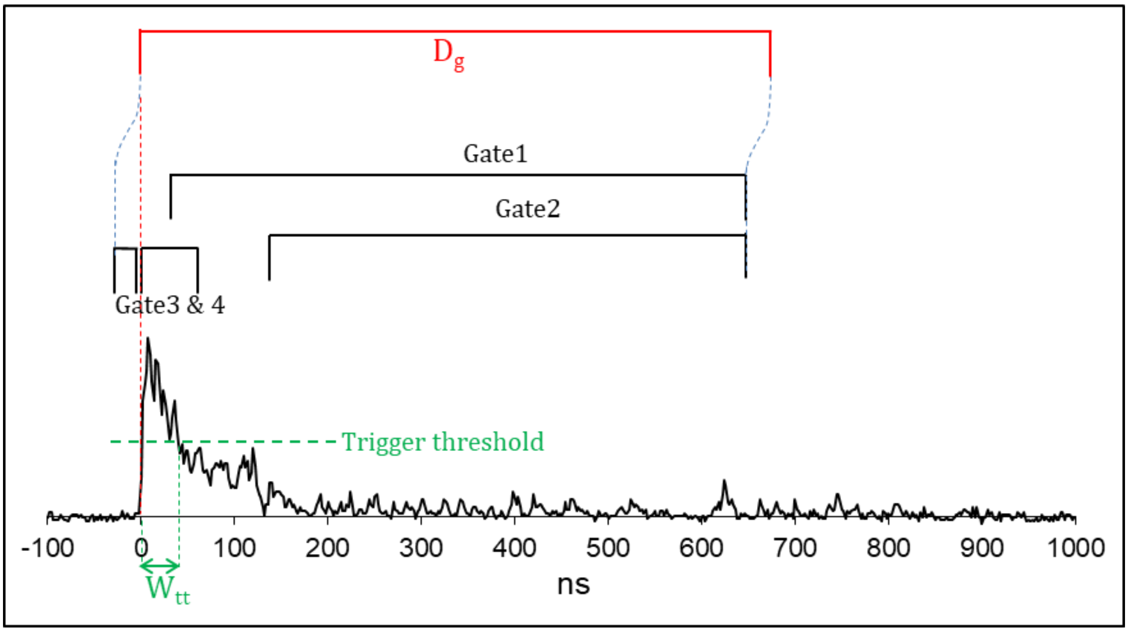

Figure 55: Dead time of the QDC data. Definition of the pulse width W_{tt} and the maximum gate duration D_g.

$$DT_{QDC} = \max(W_{tt} + 2\,ns, D_g)$$ **Equation III-1**

The user must take care to buffer depth of the computer. He can then check the match between the stored data number with myChannel_CALC and myChannel_SENT.

III.H.2 Dead time of the counting data

III.H.2.a myChannel_CALC

The dead time of the event counted in myChannel_CALC is equal to DT_{QDC} (cf. Equation III-1).

III.H.2.b myChannel_SENT

The dead time of data sent to computer depends of the data rate and the depth of FPGA buffers.

If the data rate is too high for FASTER acquisition, typically above 500 000 events per second, the dead time is not constant. It is equal to DT_{calc} at the beginning, (typically the first 10 s if the rate is under 3.10^6 events per second). As soon as the FIFO are full, all the data of all the channel belonging to the same µTCA carrier are sent with the rate of the Gigabit Ethernet communication. The FIFO are emptied in turn and a constant dead time is not guaranteed. The experimenter can increase the “QDC_TDC” data decimation in order to reduce the rate of the sent events. He must likewise disable the sending of the oscilloscope data, or reduce the number of samples of the oscilloscope data frames.

III.H.3 Dead time of the “Oscillo” data

The dead time of an oscilloscope frame is

$$DT = fullscale_X + 88 \text{ ns}$$ **Equation III-2**

$fullscale_X$ is defined in chapter III.A.4 .

IV First experience with The QDC-TDC MnM

Or "how to adjust the QDC-TDC instrumentation module"

This chapter describes step by step, how to adjust the FASTER V2 – FASTER GUI (QDC-TDC) Config parameters, by doing the ^{137}Cs source spectrometry. The detector XP2060B (Saint-Gobain Crystals) used is composed of a LaBr scintillator coupled to a PMT

We will use a dynamic BLR and a threshold discriminator.

IV.A Preliminary Step

You have previously run on your terminals:

```
~/ your_work_directory/faster_gui
~/ your_work_directory/RF_RHB_Demo/full_config/RHB -r
```

You may use an "Oscilloscope" display and a "Spectrum" display of the channel you want to adjust.

Click on the "Start" button on the FASTER GUI application. Start displaying on `RHB -r`.

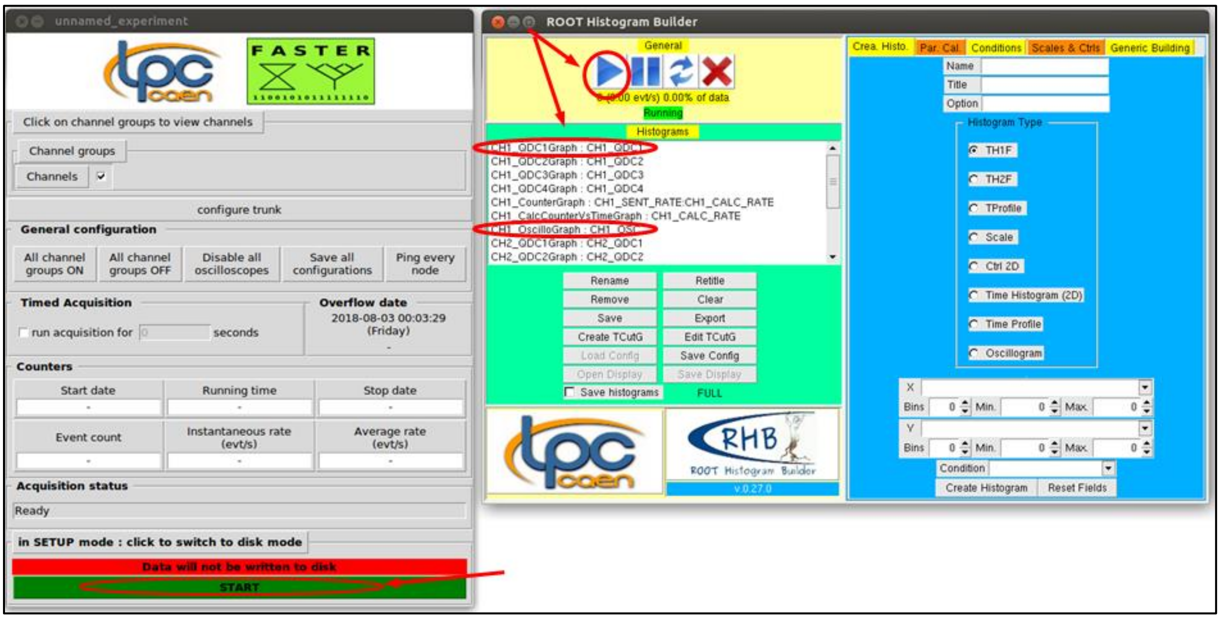

Figure 56 : Start the acquisition, start displaying.

IV.B Input parameter selection

It is important to inspect the input signal of the QDC-TDC MnM to adjust the input dynamic range and to verify that the signal from the analogic-to-digital converter is not saturated. To do that, you must inspect the raw signal with the Oscilloscope module. Refer to section III.B.2 and III.B.3 for more information.

<u>Step 1:</u> Adjust the oscilloscope parameters

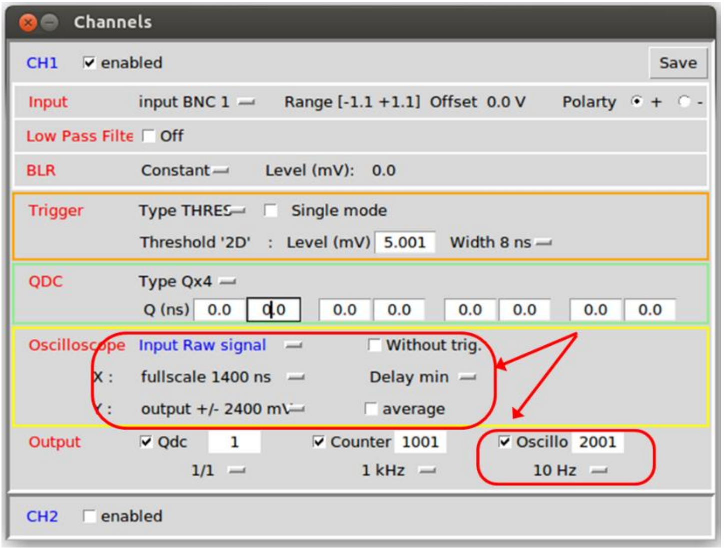

Figure 57: Oscilloscope tunings to inspect raw signal

You may tune the oscilloscope parameters as shown on Figure 57, i.e.:

- Oscilloscope input: "Input Raw signal";
- Time fullscale 1400ns;
- Y-fullscale: the greatest proposed fullscale. That means +/-2400mV;
- "Without Trig" mode checked, in order to display the signal, even if the trigger module has not been adjusted;
- "Output Oscillo" enabled with a 10Hz frequency.

<u>Step 2:</u> Inspect the input raw waveform

For example, here is the obtained graph.

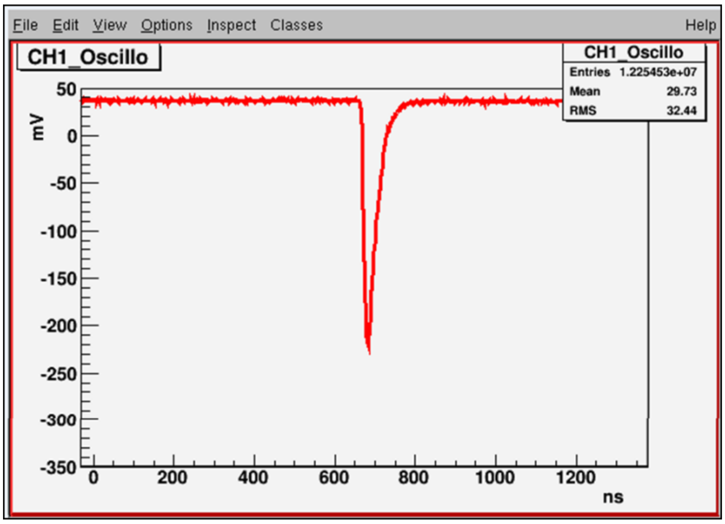

Figure 58: Example of an input raw signal graph

You are now able to establish the signal polarity. The polarity is here negative.

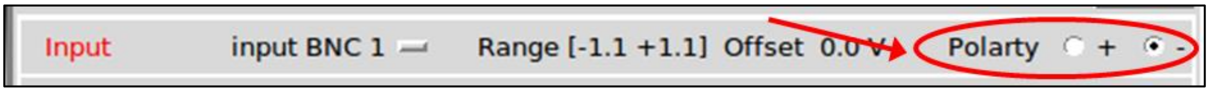

Figure 59: The polarity parameter

If the event flow is low, you should increase the "oscilloscope X fullscale" configuration to try displaying an event pulse in "Without Trig." mode

You are able to define an approximate baseline level. Choose the best dynamic range scale to be sure that pulses are not saturated.

Use a positive offset if the signal polarity is negative and a negative offset if the signal polarity is positive. But if possible, let the offset to zero because this configuration is the less noisy.

In our example, by adding 1V, the raw data baseline will be set around 1V, and the input data could have a 2V-excursion.

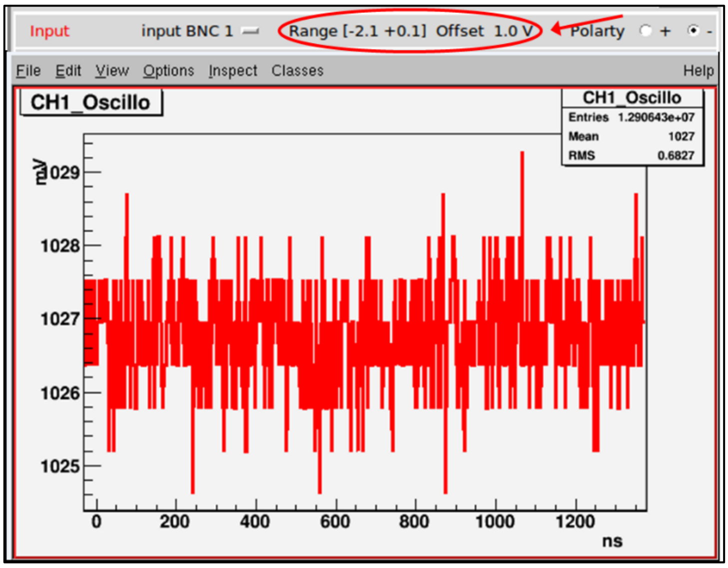

Figure 60: Input range adjustment

IV.C The BLR parameter selection

The "Constant BLR" is very easy to configure (select first "Constant BLR" in the BLR module; fill in the "level" value with 0; display then the "Input Constant BLR" oscilloscope channel in "Without Trig." mode; and finally fill in the "level" value with the signal mean value shown on the display:here is -1026.8 mV).

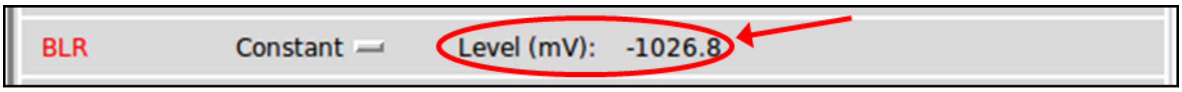

Figure 61: Constant BLR adjustment.

That's why we will rather explain in more detail how to adjust the dynamic BLR. Refer to the "Dynamic BLR" section p18 for more information.

<u>Step 3:</u> Adjust the oscilloscope parameters.

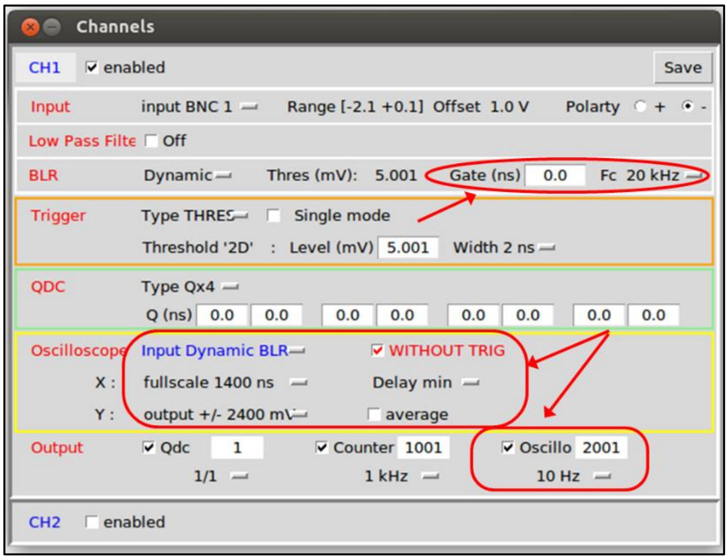

Figure 62: Oscilloscope tunings to inspect Dynamic BLR signal

You may tune the oscilloscope parameters as shown on Figure 62, i.e.:

- Oscilloscope input: "Input Dynamic BLR"
- Time fullscale 1400 ns;
- Y-fullscale: +/- 2400 mV;
- Average parameter: any settings are equivalent.
- "Without Trig" mode first checked.

Step 4: Fill in first 0 ns in the "Gate" parameter, and select 20 kHz for the cut-frequency as shown on Figure 62.

Step 5: On the un-triggered "Input Dynamic BLR" graph (Figure 63), note the noise peak level.

Here we have $|V_{noise\text{-}peak}|$=3.4 mV.

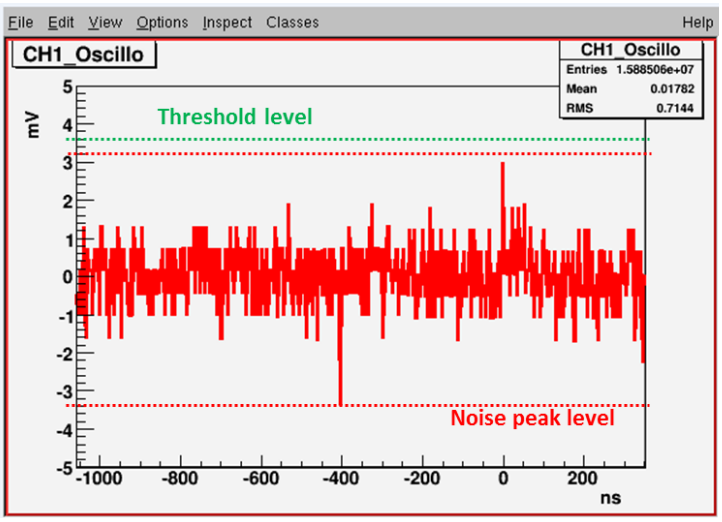

Figure 63: noise peak level

By unchecking now "Without trig" in the oscilloscope module, try to find the lowest trigger threshold V_{thr} which triggers on an event, and doesn't trigger on the noise.

In our example, V_{thr} = 3.8 mV.

Step 6: Adjust the BLR Gate: this gate represents the time when signal is under the threshold level, but the samples still belong to the event pulse.

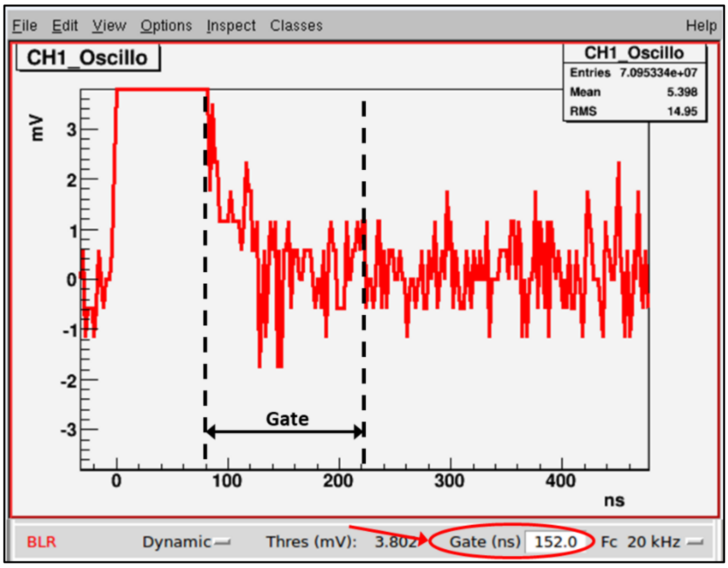

Figure 64: the "BLR Gate" parameter

⚠ When determining the gate width, use a high-amplitude signal, in order to be sure that the end of the pulse is long enough above the noise.

Step 7: Depending on the EMC and the data flow, eventually increase the BLR cut-off frequency.

Step 8: You can inspect the signal EMC, by increasing the oscilloscope X-fullscale.

IV.D The QDC module parameter definition

Step 9: Select the charge number. Here, we need only one charge Qx1.

Step 10: Inspect the "input QDC" signal with the oscilloscope to define the charge integration gate parameters.

In order to inspect the "input QDC" signal, tune the oscilloscope parameters as shown Figure 65, i.e.:

- Oscilloscope input: "Input QDC DSP";
- Time fullscale 1400 ns ;
- Y-fullscale: +/- 2400 mV fullscale or less depending on signal amplitude;
- Average parameter: unchecked;
- Delay min.

You can choose 1Hz as the oscilloscope output frequency, and check "Single mode" if you prefer.

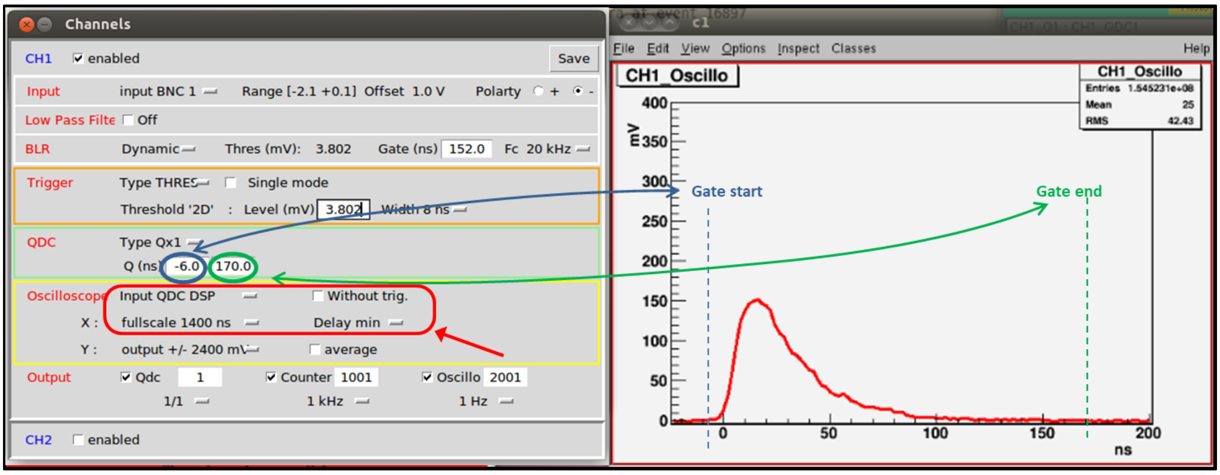

Figure 65: oscilloscope tunings to inspect signal which will be integrate, and gate definition

Step 11: Display the charge spectrum with RHB

⚠ You should display with an adequate spectrum resolution.

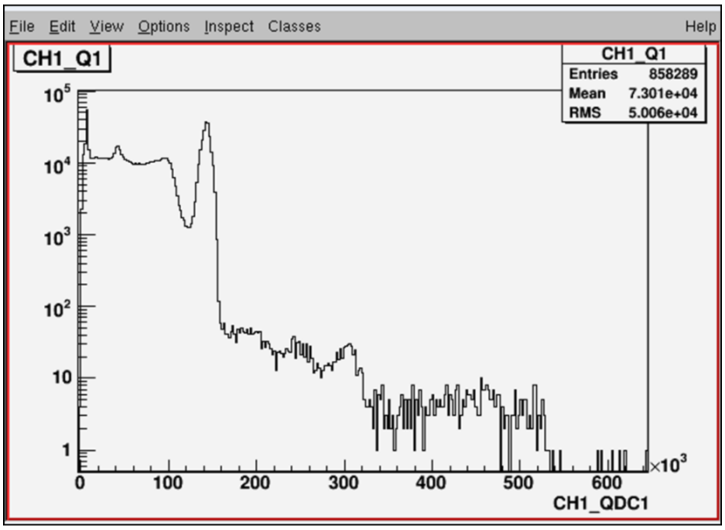

Figure 66: ^{137}Cs spectrum

Step 12: Reajust "Trigger" module parameters if desired :

Step 13: If better, you can increase "Trigger Threshold" Width, decrease a little "Trigger Threshold" Level, and use a filtered input signal.

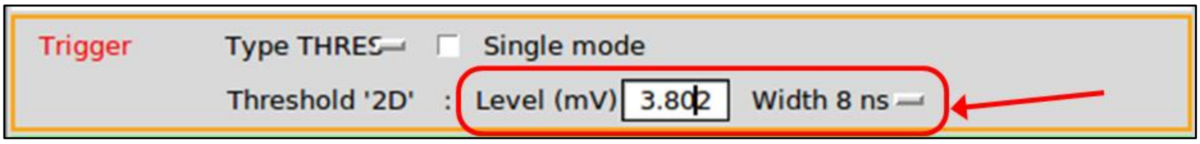

Figure 67: "Trigger module" Threshold '2D' parameters

⚠ In case of dynamic BLR, if the trigger Threshold '2D' is below the BLR threshold, the charge calculation of the signal, whose amplitude is under then BLR threshold, may be undervalued. Signals under or above BLR threshold did not undergo the same signal processing.

Step 14: Click on the "Save" button to prevent from loss of your settings.

PARAMETER AZ index