

FASTER CRRC4-Spectro MnM USER MANUAL

This document is the user manual of the FASTER CRRC4-Spectro MnM (Measurement numerical Module). The CRRC4 Spectro MnM is a spectroscopy module.

In chapter one, you will find an introduction to the spectroscopy chain.

In chapter two, all tuning parameters of the FASTER CRRC4-Spectro MnM are described.

In chapter three, a FASTER CRRC4-Spectro tuning procedure is suggested.

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Theory of operation

A spectrometer is an instrumentation system designed for the measurement energy spectra of radiations. This system includes the essential modules shown in Figure 1.

Ι



Figure 1: Essential modules in a spectroscopy set-up.

The charge preamplifier amplifies the signal from the detector. The CRRC4-Spectro MnM contains all the set of modules used for spectroscopy. The signal from preamplifier is digitalized. Therefore, the signal processing is digital.

I.A Charge Preamplifier

The preamplifier transforms signal from the detector as follows:



Figure 2: Signal from charge preamplifier

The gain of the charge preamplifier is fixed by an internal capacitor. In order to avoid exceeding the dynamic range of the following circuit, the preamplifier contains a resistor. The capacitor-resistor define the characteristic time constant of the charge preamplifier τ_{cap} . This time constant τ_{cap} adds a pole in the signal processing equation. This pole must be canceled by the following signal processing.

I.B FASTER CRRC4-Spectro Signal Processing

The CRRC4-Spectro MnM is able to handle charge preamplifiers with a time constant from about 8µs up to about 600µs (depending on the chosen processing shaping time).

The input dynamic range of FASTER CRRC4-Spectro MnM depends on the daughter card installed in the module.

The CARAS daughter card dynamic range is +/-1.2V. The dynamic range can be shifted by adjusting an offset. The CARAS daughter card has to be used in its high impedance configuration. On the CARAS daughter card, there are two input channels.

For the MOSAHR daughter card, the dynamic range is either +/-1V, +/-2V, +/-5V or +/-10V. On the MOSAHR daughter card, there four input channels.

II Preamble

II.A FASTER launching

To take benefit of the "CRRC4" spectroscopy of the FASTER acquisition, the experimenter can build his experiment interface with the command faster setup gui.

The interface, shown on Figure 3, is launched. To use the FASTER CRRC4 -Spectro MnM, the experimenter must select the "CRRC4 Spectro" type, by right-clicking on the daughterboard line.

😣 🗐 🗊 🛛 FASTER setup G	UI						
Experiment settings Name unnamed_experime t0 target 192.168.1.204	nt 192.168.0.1 02.168.0.2	Specific MNM opt Trapezoidal spe	ions ctrometry expe	rt mode	F A S T E		
Component	na	me	data label	group	ip address	Status	-
	noname				192.168.1.204	ok	
NotUsed:null node	daughterboard	A daughterboard / change measure	A ement type ျ⊧	CARAMEL MOSAHR HV NotUsed CARAS	CRRC4 Spectro Trapezoidal Spec	ok ctro	×
-Command panel (right click to Channels (0 channels)	add or edit chanr	cor nel group)	mmand panel			`	

Figure 3: Experiment building with "faster_setup_gui".

Before exiting the application form, the user can choose the names of the experiment, of the daughterboard and of each channel of the daughterboard.

With the command line faster_gui, the experimenter accesses to the FASTER acquisition display, shown on Figure 4.

🗕 unnamed_e	xperiment			
Click on channe	l groups to view cha	annels		
Channel group	s			
Channels	-			
	t	rigger-merger configura	ation	
General configur	ation			
All channel All channel Disable all groups ON groups OFF oscilloscopes		Save all configurations	Ping every node	
Timed Acquisitio	n or o seco	onds	Overflow date	-
Counters				
Start da	ate	Running time	Sto	op date
•	1			-
Event co	unt	Instantaneous rate (evt/s)	Aver	age rate evt/s)
		•		•
Acquisition status	• · · · · · · · · · · · · · · · · · · ·			
Ready				
in SETUP mode :	click to switch to	disk mode		
	Data	a will not be written i	to disk	
		START		

Figure 4: faster_gui interface.

By clicking on "Channels" (cf. Figure 4), the MnM interface is displayed, allowing the user to adjust the different module parameters.

Figure 5 shows the FASTER CRRC4-Spectro MnM interface:

😣 🖨 Chann	els
CRRC4_SPEC	TRO_1 vee enabled
Input	SMB 1 🛁 +/- 5V Range switches match Polarity 🖲 + 🔾 -
Subtraction	Base line level (mV) 0.0
Fast Out	Shaping Time 💿 25ns 🔿 60ns
Spectro Out	Shaping 2 µs - Pole-Zero(µs) 8.129 Unipolar -
	Dynamic BLF F HighFc Thr(mV) 0.6 Gate(µs) 22.09€ Auto
Trigger	Threshold — Input Fast Out 🛁 🗌 Single mode
	Threshold '2D' : Level (mV) 0.8 Width 8 ns 💻
ADC	Input Spectro Out — Width (µs) 22.096 V Auto
Oscilloscope	Input Raw signal 🛁 🗌 🗆 Without trig.
x :	fullscale 6000 ns 🛁 🛛 Delay min 🛁
Y:	+/- 150 mV 🛁 🗌 average
Output	ADC 1 Counter 1001 Oscille 2001
	1 Hz 🛁 10 Hz 🛁

Figure 5: CRRC4-Spectro interface

II.B RHB launching

To take benefit of RHB displays, the experimenter shall execute the command faster_rhb_demo_crrc4_spectro_copy in the working directory, in order to have an example of RHB files adapted to the FASTER CRRC4-Spectro MnM.

A new repertory ADC_RHB_Demo is created. The user shall go in the full_config repertory contained in the repertory ACD_RHB_Demo, before launching RHB interface.

```
cd ADC_RHB_Demo
cd full_config
RHB -r
```

III FASTER CRRC4-Spectro MnM Description

The CRRC4-Spectro MnM is a signal processing designed for signals digitalized by a 14-BIT, 125MHz analogic-to-digital converter. That means that the module receives a 14BIT-sample every 8 ns, and is able to timestamp its output data with an accuracy of 8 ns. Nevertheless, the timestamp LSB value is 2 ns. That means that every event timestamp value has to be multiplied by 2 ns to have event date in nanoseconds.

The FASTER-ADC module contains the following elements:

- A dynamic range tuning (depending on FASTER daughter card),
- A polarity tuning,
- Three shapers modules which operate in parallel,
- A trigger module,
- An ADC module: amplitude peak-hold module,
- An oscilloscope,
- An event counter.

It is important to know the role of each element in order to obtain energy spectra with the best resolution.

The FASTER -ADC module provides three kinds of 8ns-accuracy dated data:

- Oscilloscope data
- ADC data
- Event counter data.

This data can be displayed thanks to the Root Histogram RHB.



The FASTER CRRC4-Spectro MnM structure of processing is shown below.

Figure 6: Diagram of the FASTERCRRC4-Spectro signal processing..

III.A The Oscilloscope module

The oscilloscope displays the signal at the output of the various modules described later.

▲ It is not calibrated, and the scale in millivolts of the y-axis is only an indication of the voltage.

Nevertheless, the FASTER oscilloscope includes several features found on any ordinary oscilloscope, like trigger choice, channel display choice, horizontal tuning, and vertical tuning. Additionally, FASTER-ADC processing lets you select acquisition speed.

III.A.1 The oscilloscope trigger choice



Figure 7: The trigger mode parameter

The oscilloscope display can be triggered by the discriminator module or not. During the initial settings, it's very useful to select "Without trig.". This tuning helps to identify the shape of the signal, and its polarity.

III.A.2 The oscilloscope input channel



Figure 8: The inspected channel

The oscilloscope displays several signals from different modules:

- "Input Raw Signal": The FASTER daughter card includes an analogic-to-digital converter. This channel shows data digitalized by this converter.
- "Input Subtraction": This channel shows data from subtraction shaper module. Refer to section III.C.1 .
- "Input Fast Out": This channel shows data from "Fast Out" shaper module. Refer to section III.C.2 .
- "Input Spectro Out": This channel shows data from "Out" shaper module. Refer to section III.C.3
- "Input BLR B.Line": This channel shows the baseline of "Out" data filtered by the processing unit. Refer to section III.C.3.d .

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III.A.3 The oscilloscope horizontal tuning

The time base of the signals can be adjusted with 3 parameters: shift, fullscale, subsampling.

III.A.3.a The horizontal fullscale



Figure 9: The horizontal fullscale parameter

The user can select between 9 fullscale ranges from $6\mu s$ to 1.4ms.

A signal graph contains 704 samples.

The time interval between two samples is: 8 ns for 6 μ s fullscale range; it is the sampling period of the 125MHz analogic-to-digital converter. The time interval is 16 ns for 11 μ s fullscale range, 32 ns for 23 μ s fullscale range, 64 ns for 45 μ s fullscale range, 128 ns for 90 μ s fullscale range, 256 ns for 180 μ s fullscale range, 512 ns for 360 μ s fullscale range, 1024 ns for 0.7 ms fullscale range, 2048 ns for 1.4 ms fullscale range.

III.A.3.b The subsampling mode



Figure 10: Oscilloscope subsampling mode

As the number of samples is constant, the time interval between two samples is different according to the horizontal fullscale. When this time interval is greater than 8 ns, there are two ways to subsample the signal:

- Either every sample of the oscilloscope display represents the average of several samples. It's the "average" mode.

- Or every sample of the oscilloscope display represents one sample every N samples. It's the "subsampling" mode.

Men a very short signal must be displayed, don't forget to change the horizontal fullscale to 6 μs fullscale. In "average mode", the average of a very short signal within a lot of samples is almost zero. In "subsampling mode", the sample shown is not necessarily the peak sample of the short signal. Therefore, a short signal exits, but it can be not-displayed.

III.A.3.c The delay

Oscilloscope	Input Spectro Out 🛛 🛁	🗆 Without trig.
X :	fullscale 6000 ns 📃	Delay min 🖃
Υ:	output +/- 1200 mV	average



This parameter is available only when the oscilloscope display is triggered by the discriminator module.

The sample, that satisfies the discriminator module conditions, is set at the very beginning (delay min), 25%, 50% or 75% of the display.

▲ The sample, which satisfies the discriminator module conditions, is always placed at abscissa "0 ns" in "X fullscale 1400ns, Delay min" configuration. It is not necessarily the beginning of the signal. If "X fullscale" and "Delay" is different from "X fullscale 1400ns, Delay min", the oscilloscope display may have a time shift.

III.A.4 The oscilloscope vertical tuning



Figure 12 : Vertical fullscale

The values of the oscilloscope samples are always signed 16 BIT values, centered on 0.

The CRRC4-Spectro MnM is processing 14 BIT signal samples. Depending on the chosen daughter card and the selected, dynamic range, fullscale is different.

For the CARAS daughter card: There are 14 BIT a fullscale around 2.4V peak to peak. But, as the signal is not 0-centered, the processing module uses 15BIT for +/-2.4V fullscale.

For the MOSAHR daughter card: There are 14 BIT for around+/-1.27V, +/-2V, +/-5.3V or +/-10.4V, depending on the switch selection on MOSAHR.

In order to perform high-resolution calculations in the processing, 7 BIT are added as accuracy BIT on the signal sample.



Figure 13: Data representation in the processing module.

The values of the oscilloscope module have only 16 BIT. Several oscilloscope fullscale ranges are available to make the most of the maximum accuracy, or of the maximum fullscale of the CRRC4-Spectro MnM.



Figure 14: The oscilloscope fullscale ranges.

For the CARAS daughter card, you find 8 fullscale choices from $\pm 2400/64 = \pm 37$ mV up to ± 2400 mV.

For the MOSAHR daughter card, you find 7 fullscale choices from Y-fullscale/64 up to Y-fullscale.

The oscilloscope fullscale range does not affect the internal representation of signal used by the module.

III.A.5 The oscilloscope acquisition speed

Output	ADC	1		✓ Oscillc 2001
			1 Hz 🛁	10 Hz -

Figure 15: The acquisition speed parameter.

There are 4 choices of acquisition speed:

- One acquisition every millisecond: 1 kHz,
- One acquisition every 10milliseconds: 100Hz,
- One acquisition every 100 milliseconds: 10Hz,
- One acquisition every second: 1Hz.

III.A.6 The "output enable" parameter



Figure 16: The oscilloscope "enable" parameter.

The oscilloscope data is only sent to the acquisition chain if the "enable" parameter is checked.

III.B The Input module

III.B.1 Channel selection

The CARAS daughter board has two input channel called SMB 1 and SMB 2.

The MOSAHR daughter board has four input channel called SMB 1, SMB 2, SMB3 and SMB4.



Figure 17: Multiplexers to select which analog channel to be processed with a CARAS daughter board.

Each FASTER CRRC4-Spectro MnM in the FPGA can be linked with any SMB, as shown on Figure 18

And and a second	DNG 1	Depart [0] ()] Offert] 0 V Deletty G ()
input	BNC 1	Range [-0.1 + 2.1] Offset -1.0 V Polarty • + •
	BNC 1	CAPAS Channels
	BNC 2	CARAS Citalineis
	Dire 2	·
Input	SMB 1	+/- 5V Range switches match Polarity 🖲 + 🔿 -
	SMB 1	1
	51-10 1	MOCAUD Channels
	SMB 2	I WOSAHR Channels
	SMB 3	1
	CMD 4	1
	SMB 4	

Figure 18: Input range adjustment for CARAS and MOSAHR daughter card

III.B.2 Range Tuning

When tuning the dynamic range, it is important to display the raw data (that means the data digitized by the converter) with the "Oscilloscope" module.

III.B.2.a CARAS daughter board

Each SMB channel can have a different dynamic input range from [0.0 + 2.2] V to $[-2.2 \ 0.0]$ V. This dynamic range is configured by the user, by clicking on "Range" switch. A new interface is launched (cf. Figure 19): the user can add a voltage source (called "Offset") between -1.1 V and 1.1 V with 0.1 V-step.



III.B.2.b MOSAHR daughter board

Each SMB channel can have a different input fullscale range from $\pm 1V$ to $\pm 10V$, set by four mechanical switches on the daughter board. By clicking on "Range switches match", a new interface is launched (cf. Figure 20), the user has to match the fullscale range of the oscilloscope display with the real electronical fullscale range.



Figure 20: fullscale range interface for MOSAHR daughter board.

III.B.3 Polarity Tuning

			MOSAHR
Input	SMB 1	- +/- 5V	Range switches match Polarity 💿 + 🔿 -
			CARAS
Input	BNC 1	-	Range [-0.1 +2.1] Offset -1.0 V Polarty • + •

Figure 21: The polarity parameter

The CRRC4-Spectro process uses positive values. If the detector provides a negative signal, it is essential to convert it into a positive signal.

III.C The Shaping module

The Shaping module includes three shapers, which operate in parallel. There are:

- The "Spectro Out" module
- The "Fast Out" module
- The "Subtraction" module



Figure 22: Shaper modules and match with the MnM GUI

The "Subtraction" is designed for the users who use an external spectroscopy module and who want make the most of FASTER acquisition.

The "Fast Out" module generates a signal with worse signal-to-noise ratio, but it is faster. It can be used to timestamp the radiation event pulses.

The "Spectro Out" module generates a signal with the best signal-to-noise ratio, provided that the user has properly set the ideal parameters.

III.C.1 The "Subtraction" module



Figure 23: The "Offset Subtraction" module.

As previously mentioned, this shaper is designed for the users, who want to use an external spectrometry module, while enjoying the FASTER acquisition convenience.

You can fill in this parameter with the DC level L_{DC} of the signal from "Polarity tuning module", to set baseline level to zero. It could be afterwards convenient, in order to easily adjust "Pole-Zero Cancellation" parameter. Refer to "Pole-Zero Cancellation" section.

III.C.2 The "Fast Out" module

The "Fast Out" module includes a unique CR-RC⁴ filter. Two high cut-off frequencies are available, and they define two different shaping times:

- σ = 25ns if "25ns" parameter is checked,
- σ = 60ns if "60ns" parameter is checked.



Figure 24: The "Fast Out" shaping time parameters.

▲ As far as possible, use the 25ns Fast Out shaping time. The timestamp will be better. But sometimes, the "25ns Fast Out shaping time" signal is too noisy to use it in the following trigger module.



Figure 25: A "Fast Out" signal. There is no Pole-Zero cancellation.

III.C.3 The "Spectro Out" module

The "Spectro Out" module is intended to filter the signal from the charge preamplifier in order to improve the signal-to-noise ratio. The implemented filter is a CR-RC⁴ filter.

The "Spectro Out" module includes the different elements shown below:



Figure 26: Out Shaper elements

In the following sections, every element is going to be described.

III.C.3.a The Pole-Zero cancellation

Spectro Out	Shaping 1 µs — Pole-Zero(µs) 60.0 Unipolar —
	Constant BLF Base line level (mV) 0.84

Figure 27: Pole-Zero cancellation parameter.

The charge preamplifier located close to the detector introduces a pole in the processing chain (time constant = τ_{cap}). It is necessary to cancel this pole with a zero. That means to cancel time constant τ_{cap} by time constant τ_{PZ} , i.e. $\tau_{PZ} = \tau_{cap}$.

In fact, the signal duration after CR-RC⁴ filter is smallest when the input CR-RC⁴ filter signal is a Heaviside function, whereas the signal from the charge preamplifier is an exponential function.

If the Pole-Zero parameter is below the time constant of the charge preamplifier, the resulted signal after CR-RC⁴ filter is overcompensated.



Figure 28: Overcompensated PZ TPZ> Tcap

If the Pole-Zero parameter is above the time constant of the charge preamplifier, the resulted signal after CR-RC⁴ filter is undercompensated.



Figure 29 : Undercompensated PZ TPZ< Tcap

If Pole-Zero parameter is equal to the time constant of the charge preamplifier, the resulted signal after CR-RC⁴ filter is well compensated.



Figure 30: Correct PZ $\tau_{PZ} = \tau_{cap}$

- A When adjusting the Pole-Zero parameter, "dynamic baseline restorer" must be disabled (that means "constant baseline restorer" must be enabled).
- ▲ When adjusting the Pole-Zero parameter, unipolar parameter (section III.C.3.c) must be selected.
- When adjusting the Pole-Zero parameter, it is convenient to know the DC level L_{DC} of the signal from the "Polarity tuning" module. This level is due to the voltage offset from the analogic stage. This DC level exists after the CR-RC4 filter, but it is attenuated by a factor depending on the shaping time and the zero-pole compensation. In the FASTER V1 – FASTER GUI (ADC) Config, when you specify L_{DC} in the "Base line level (mV)" parameter in the "Subtraction" module, the baseline level after the "Output filter" module ("Constant BLR baseline level") is automatically calculated. Reciprocally when you fill in the "Constant BLR baseline level" parameter, the "Subtraction Base line level (mV)" parameter is readjusted. The "Constant BLR baseline level" parameter is readjusted too when the "Pole-Zero Cancellation" parameter or the "CR-RC4 filter shaping time" parameter are changed. Thus, the resultant baseline level remains to zero, and it is more convenient to tune the Pole-Zero parameter when watching a zero-centred oscilloscope display.



Figure 31: Select constant BLR, and specify Base line level to help for Pole-Zero cancellation adjustment.

▲ If the signal can't be compensated by the adjustment of the pole-zero cancellation, the signal from the charge preamplifier is probably not exponential. The baseline restorer module could help to catch up the baseline level, and to compensate the Zero from the preamplifier, but the spectrometry will be worse.

*III.C.3.b CR-RC*⁴ *filter: the shaping time parameter*



Figure 32: Shaping time parameter

The essential filter of this spectrometry chain is a CR-RC⁴ filter. Several filter time constants τ_F are available, and they define several resulting shaping times.

The user can select between 10 shaping times. The shaping time represents the standard deviation of the resulting filtered signal. The best shaping time maximizes the signal-to-noise ratio and provides the best spectra resolution. The best shaping time only depends on the detector and the charge preamplifier.



Figure 33: Shaping time parameter

III.C.3.c Output mode Selection



Figure 34: Output mode parameter

After the CR-RC4 filter, you can activate a differentiator circuit, and obtain a bipolar output, instead of a unipolar one.



Figure 35: Unipolar and bipolar signal.

▲ Spectroscopy based on bipolar shaping gives worse results than with unipolar shaping, but is less sensitive to pile-up.

III.C.3.d Baseline restorer

There are two kinds of baseline restorer:

- A constant baseline restorer,
- A dynamic baseline restorer.

The constant baseline restorer



Figure 36: Constant level subtraction

This baseline restorer simply subtracts a constant level.

The dynamic baseline restorer

This baseline restorer follows the slow variations of the signal baseline.



Figure 37: Dynamic baseline restorer parameter

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Theory of operation:



The theory of operation of the baseline restorer is shown below:

Figure 38: Theory of operation of baseline restorer: Threshold, Gate and Fc have to be tuned.

The "Out" signal of the "Spectro Out" module is filtered by a low-pass filter. This filter lets through any slow variations of the signal. The **cut-off frequency Fc of this low-pass filter** is either 610Hz, if the "HighFc" parameter is unchecked. It depends on the shaping time if the "HighFc" parameter is checked. It is 1.3 MHz for the 60 ns shaping time, 640 kHz for the 125 ns shaping time, 320 kHz for the 250 ns shaping time, 160 kHz for the 500 ns shaping time, 80 kHz for the 1 μ s shaping time, 39 kHz for the 2 μ s shaping time, 19 kHz for the 4 μ s shaping time, 10 kHz for the 8 μ s shaping time, 4.9 kHz for the 16 μ s shaping time, 2.4 kHz for the 32 μ s shaping time.

The baseline tracking by the low-pass filter is stopped when an event is detected **during a duration defined in the "Gate" parameter**. That means when a "**Fast Out" sample exceeds a** "**threshold**" **parameter value**. When the baseline tracking is stopped, the computed baseline value is equal to the baseline value just before the detected event. In case of pile up, the computed baseline value is equal to the baseline value just before the first detected event.



Figure 39: Focus on the BLR signal

 \triangle It is important to properly adjust the automatic baseline restorer: that means adjust the threshold "Thr(mV)", the cut-off frequency "High Fc", and the duration "Gate".

Dynamic baseline restorer adjustment:

The BLR threshold:

When tuning the BLR threshold, you must inspect the "Fast Out" signal with the internal oscilloscope. The threshold level should be chosen just above the noise. The danger of setting the BLR threshold too high is that an event may be considered as a baseline, and the dynamic baseline restorer is incorrectly adjusted.



Figure 40: Baseline restorer threshold tuning

- Dynamic BLR discriminator operates as the threshold trigger of "Trigger" module if the following conditions are satisfied in "Trigger" module (refer to §III.D):
 - "Threshold" is selected;
 - "Input Fast Out" is selected;
 - 8 ns "Width" is selected.
 - The "Trigger" Threshold level is the same as the "BLR" Threshold level.

It is then convenient to inspect the "Input Fast Out" oscilloscope channel. By simultaneously and gradually increasing the "Trigger" and the "BLR" threshold levels, the user can easily find the lowest level which discriminate an event.

The BLR cut-off frequency:

When tuning the cut-off frequency, it is always better to uncheck "HighFc". Thus, you work with the lowest 610Hz cut-off frequency. In this configuration, the baseline restorer module generates less noise. But depending on the EMC shielding of the detector/preamplifier, "HighFc" can sometimes give better results.

BLR gate:

To tune the "Gate" parameter, you must inspect "Spectro Out" signal with the internal oscilloscope. "Gate" represents "Spectro Out" signal duration. Nevertheless, the MnM GUI provides some Gate values, which are adapted to the chosen shaping time if "Auto" parameter is checked.

Spectro Out	Shaping 1 µs — Pole-Zero(µs) 60.0 👌 Unipolar —
	Dynamic BLF HighFc Thr(mV) 0.599 Gate(µs) 11.0 V Auto

Figure 41: The automatic gate parameter

▲ If the baseline restorer is incorrectly adjusted, the resulting spectroscopy could be disastrous. You should use the constant BLR.

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III.D The "Trigger" module

The "Trigger module" mainly includes a threshold discriminator. But the CRRC4-spectro processing can use an external trigger. When an event is detected by the trigger module, this event is timestamped with a 8ns accuracy clock.

III.D.1 Internal or External Trigger



Figure 42: Internal or external trigger

There are many CRRC4-spectro MnMs implemented in one FPGA on the mother card. Each MnM has an internal trigger, but a MnM can use the trigger of the adjacent MnM (cf. Figure 43) by checking "External"



Figure 43: Crossed trigger diagram

III.D.2 The input signals



Figure 44: Internal trigger input signals

The "Trigger" module can select one of the three signals from the "Shapers" module, as shown in Figure 44.

- Either the signal from the "Subtraction" channel,
- Or the signal from the "Fast Out" channel,
- Or the signal from the "Spectro Out" channel.
- ▲ If possible, select the "Fast Out" channel as trigger signal: the timestamp accuracy will be better! But, as the spectroscopy channel has a better SNR, you will detect lower pulses by selecting "Spectro Out".

III.D.3 The single mode

Trigger	Threshold 🛁		Input Fast C		Single mode		
	Threshold '2D'	:	Level (mV)	0.03	Width	8 ns	-

Figure 45: Single mode parameter.

It is sometimes convenient to trigger in "single mode" while performing the setup operation. That means that, after the first trigger found, the "trigger" module is disable. The just-emerged sample on the energy spectrum and the oscilloscope graph represent the same event. The "Trigger" module can be reactivated by clicking on "Arm" button.

Trigger	Threshold 💻		Input Fast Out 🛛 🛁	Single ARM
	Threshold '2D'	:	Level (mV) 0.03	Width 8 ns 🛁

Figure 46: Single Arm button.

▲ After setup operation performing, don't forget to uncheck "Single Mode".

III.D.4 The threshold parameters



Figure 47: Trigger conditions

Three conditions are required for the module to send a trigger signal:

- The signal sample is above the threshold defined by the user



Figure 48: Threshold level parameter.

- The triggering occurs on rising edge

- The samples are above the threshold during a time window, which has a width defined in the "width" parameter.

Trigger	Threshold 🛁		Input Fast Out 🚽 🗌 Single mode
	Threshold '2D'	:	Level (mV) 0.03 Width 8 ns -

Figure 49: Time window width parameter.

There are four choices of time window width: 8 ns, 16 ns, 24 ns and 32ns. When the 8ns width is selected, all pulses exceeding the threshold on rising edge are triggered, because the analogic-to-digital step is 8 ns. Selecting a time width above 8 ns avoids triggering on pulse spikes or noise.

▲ The event is timestamped with the sample time just after the trigger conditions occur. On all oscilloscope displays, in "X fullscale 1400ns, Delay min" configuration, this trigger time is locally set to 0 ns, instead of the timestamp value.

III.E The "ADC" module

In the MnM interface, this module is identified by "ADC".



Figure 50: Peak detection on "Spectro Out" signal.

The ADC module looks for the highest peak amplitude in a validation time gate. The time gate duration is defined by a parameter.



Figure 51: Selected peak versus validation gate.

The ADC module is reactivated 80ns after the end of the validation gate.

The "ADC" module also detects pile-up.



Figure 52: Activation of validation gate in red.

In Figure 52 two data is sent: the maximum of the validation gate 1 (i.e. MAX 1), and the maximum of the validation gate 3 (i.e. MAX 3). Both data are considered as piled-up because the process has detected the "Trigger 2".

III.E.1 The validation time gate width



Figure 53: Validation time gate parameter.

The validation time gate begins from the trigger detection and lasts for the time defined by the user in the "Width" parameter. In fact, this time width depends on the shaping time filter. The MnM interface provides this time, but checking "Manual" allows the user to choose the validation gate duration.

- ▲ The validation gate should last until the end of the input signal. If the gate is too long, some data may be flagged as piled-up, although it is not piled-up. If the gate is too short, the next peak-hold data could be flagged as "not piled-up", although it is piled-up.
- \triangle This module has a dead time of 80 ns after every validation gate.

III.E.2 The input signals of the "ADC" module



Figure 54: "ADC" input signal parameter.

The "ADC" module can be fed by one of the three signals from the "Shapers" module, as shown in Figure 54:

- Either the signal from the "Offset Subtraction" channel,
- Or the signal from the "Fast Out" channel,
- Or the signal from the "Spectro Out" channel.

▲ If possible, select "Spectro Out" channel as "ADC" input signal: spectrum accuracy will be better!

III.F Data output module

The Data output module (Figure 55) defines the output data sent to the computer by checking buttons ①. These data are:

- the data processed by the ADC module ⁽²⁾,
- the counting data (3),
- the data from the Oscilloscope module ④.

To distinguish these data in the stored file, they have different labels (5). The user can moreover control the rate of output data.



Figure 55: parameters of the Data output module

When the data comes out the FASTER CRRC4-Spectro MnM, they are temporally stored in some buffers of the FPGA, waiting for being sent to the computer by the Gigabit Ethernet communication.

Here are described the content of each data. If the experimenter uses RHB facilities, data from FASTER CRRC4-Spectro MnM are called CRRC4_SPECTRO in the RHB file "*.pid". In this file, the prefix label of each channel of the FASTER acquisition is defined. For example, if there is

1:CRRC4_SPECTRO: myChannel

that means that all data from the first channel of FASTER acquisition must have the prefix "**myChannel_**" in the configuration file of RHB (i.e. "*.facqConf" file). The "RHB –r" command, made in the directory including these files, starts RHB interface.

III.F.1 "ADC" data

The experimenter can store or display all "ADC" data processed by the ADC module by enabling data output (cf. Figure 55 ①).

In "ADC" data, the user has, for each event:



Figure 56: ADC data. The flags saturated and pileup are not displayed.

- **myChannel_ADC**: the amplitude of the OUT signal. myChannel_ADC is a 22-BIT signed integer. If the module doesn't find a maximum in the validation gate, it sends -2097152.
- **myChannel_max_dt**: the location in nanosecond of the maximum amplitude of the pulse.
- **myChannel_pileup**: the piled-up event flag. The value 1 indicates that the event is piled-up.
- **myChannel_saturated**: the saturation flag. The value 1 informs that the raw signal, that has generated the ADC signal, is outside the input range of the daughter card.
- **myChannel_t**: the time-stamp (in nanosecond) of the event, with an 8 ns accuracy.

III.F.2 "Counters" data

The experimenter can store and display the counting data, called "Counters" with a selected frequency of 1 Hz, 10 Hz 100 Hz and 1 kHz.

Output	ADC	2	Counter 1002	✓ Oscillc 2002	
			1 Hz -	10 Hz 🛁	
-	_		1 kHz		_
			100 Hz		
			10 Hz		
			1 Hz		

Figure 57: out frequency of the "Counters" data

Each "Counters" data has:

- myChannel_COUNT_t: the time-stamp of the "Counters" data
- **myChannel_TRIG**: the number of events discriminated by the Trigger module of the MnM.
- myChannel_CALC: the number of events that the ADC module has processed.
- **myChannel_SENT**: the number of data processed by ADC module, temporally stored in the FPGA buffers, and waiting for being sent to the computer.

The following inequality is always verified: myChannel_SENT \leq myChannel_CALC \leq myChannel_TRIG.

These 3 numbers are reset each time any module parameters is changing.

III.F.3 "Oscillo" data

The "Oscillo" data, already explained in chapter III.A, are defined in RHB by the variables:

- myChannel_OSC_t: the time stamp of the "0 ns" sample of the oscilloscope frame.
- myChannel_OSC: the Oscilloscope frame.

III.G Dead time

Depending on the considered data, the dead time is not the same.

III.G.1 Dead time of the counting data

III.G.1.a myChannel_TRIG

The dead time of the event discriminated by the Trigger module depends on the spreading of the input signal of the Trigger module:

 $DT_{trig} = duration of the trigger module signal + 8 ns$ Equation III-1

III.G.1.b myChannel_CALC

The dead time of the event processed by the ADC module depends on DT_{trig} and the duration of the "validation time gate" increased by 80 ns (cf. Figure 53):

 $DT_{calc} = \max(DT_{trig}, validation time gate+80 ns)$

Equation III-2

III.G.1.c myChannel_SENT

The dead time of data sent to computer depends of the data rate and the depth of FPGA buffers.

If the data rate is too high for FASTER acquisition, typically above 500 000 events per second, the dead time is not constant. It is equal to DT_{calc} at the beginning, (typically the first 10 s if the rate is under 3.10^6 events per second). As soon as the FIFO are full, all the data of all the channel belonging to the same μ TCA carrier are sent with the rate of the Gigabit Ethernet communication. The FIFO are emptied in turn and a constant dead time is not guaranteed. He must likewise disable the sending of the oscilloscope data, or reduce the number of samples of the oscilloscope data frames.

III.G.2 Dead time of the "Spectro" data

The dead time of the "Spectro" data is equal to DT_{calc} if the data rate is under 500 000 events per second. Some data can be lost otherwise

The user must take care to buffer depth of the computer. He can then check the match between the stored data number with myChannel_CALC and myChannel_SENT.

III.G.3 Dead time of the "Oscillo" data

The dead time of an oscilloscope frame is

DT = oscilloscope frame duration + 88 ns Equation III-3

In the basic mode, the oscilloscope frame duration is equal to 700 samples x 8 ns.

IV First experience with CRRC4-Spectro MnM

Or "how to adjust the CRRC4-Spectro MnM parameters"

This chapter describes step by step, how to adjust the CRRC4-Spectro parameters, by doing the ¹³⁷Cs source spectrometry. The detector used is an HPGe. It is followed by an Ortec charge preamplifier.

IV.A Preliminary Step

You have previously run on your terminals:

```
~/ your work directory/faster gui
```

```
~/ your_work_directory/RF_RHB_Demo/full_config/RHB -r
```

You may use an "Oscilloscope" display and a "Spectrum" display of the channel you want to adjust.

Click on the "Start" button on the FASTER GUI application. Start displaying on RHB -r.



Figure 58 : Start the acquisition, start displaying.

IV.B Input parameter selection

It is important to inspect the input signal of the CRRC4-Spectro MnM to adjust the input dynamic range and verify that signal from the analogic-to-digital converter is not saturated. To do that, you must inspect the raw signal with the Oscilloscope module. Refer to section III.B for more information.

Step 1: Adjust the oscilloscope parameters

😣 🖨 Chann	els
CRRC4_SPEC	TRO_1 vee enabled
Input	BNC 1
Subtraction	Base line level (mV) 0.0
Fast Out	Shaping Time
Spectro Out	Shaping 2 µs → Pole-Zero(µs) 500.0 Unipolar → Constant BLF→ Base line level (mV) 0.0
Trigger	Threshold Input Fast Out Single mode Threshold '2D' : Level (mV) 0.03 Width 8 ns
ADC	Input Spectro Out — Width (µs) 22 🗸 Auto
Oscilloscope X : Y :	Input Raw signal → ♥ WITHOUT TRIG fullscale 1.4 ms → Delay min → output +/- 2400 mV→ □ average
Output	Image: ADC Image:

Figure 59: Oscilloscope tunings to inspect raw signal

You may tune the oscilloscope parameters as shown on Figure 59, i.e.:

- Oscilloscope input: Input Raw signal;
- Time fullscale 1.4ms in order to see preamplifier signal as a whole;
- Y-fullscale: the greatest proposed fullscale. It depends on daughter card CARAS or MOSAHR;
- Average unchecked;
- "Without Trig" mode checked, in order to display the signal, even if trigger module has not been not adjusted;
- "Output Oscillo" enabled with a 10Hz frequency.

Step 2: Inspect the input raw waveform

For example, here is the obtained graph.



Figure 60: Example of an input raw signal graph

You are now able to define an approximate baseline level. Choose the best dynamic range scale to be sure that the pulses are not saturated (Figure 61)

- If the CARAS daughter card is plugged, use a positive offset if the signal polarity is negative and a negative offset if the signal polarity is positive. But if possible, let the offset to zero because this configuration is the less noisy. In our example, by adding -1V, the raw data baseline will be set between -900mV and
- 1V, and the input data could have a 2V-excursion.
 If the MOSAHR daughter card is plugged, the dynamic range scale is selected by a switch on the daughter card. Make sure that you use the good channel.



Figure 61: Input range adjustment for CARAS daughter card

You must then select the signal polarity. The polarity is here positive.



Figure 62: Tune polarity parameter

IV.C Trigger and Fast Out parameter selection

You must be sure that the "Fast Out" signal is sufficiently well-defined because this signal indicates to the baseline restorer of the "Out" module when there is an event. Refer to section III.C.2 and 0 for more information.

<u>Step 3:</u> Adjust the oscilloscope parameters.

😣 🖨 Chann	els
CRRC4_SPEC	TRO_1 vee enabled
Input	BNC 1 — Range [-0.0 +2.2] Offset -1.1 V Polarty • +
Fast Out	Shaping Time 25ns 60ns
Spectro Out	Shaping 2 µs Pole-Zero(µs) 500.0 Unipolar Constant BLF Base line level (mV) 0.0
Trigger	Threshold Input Fast Out Image: Single mode Threshold '2D' Level (mV) 0.03 Width 8 ns
ADC	Input Spectro Out — Width (µs) 22 🗸 Auto
Oscilloscope X : Y :	Input Fast Out → VITHOUT TRIG fullscale 6000 ns → Delay min → output +/- 2400 mV→ □ average
Output	Image: ADC Image: Counter IOOI Image: Oscille 2001 1 Hz 10 Hz

Figure 63: Oscilloscope tunings to inspect the "Fast Out" signal

You may tune the oscilloscope parameters as shown on Figure 63, i.e.:

- Oscilloscope input: Input Fast Out
- Time fullscale 6000 ns in order to see the narrow shape of the "Fast Out" signal;
- Y-fullscale: +/- 2400 mV fullscale for CARAS, and the greatest proposed fullscale for MOSAHR;
- Average parameter: any settings are equivalent.
- "Without Trig" mode first checked.

Step 4:Select the 25ns shaping time in the "Fast Out" section, as shown on Figure 63.Step 5:On the un-triggered "Fast Out" graph (Figure 64), note the noise peak level.

Here we have $|V_{noise-peak}|=0.4$ mV.



Figure 64: Noise peak level

By unchecking now "Without trig" in the oscilloscope module, try to find the lowest trigger threshold V_{thr} which triggers on an event, and doesn't trigger on the noise. The trigger "width" parameter should be filled in with 8ns value.

The trigger parameter settings are also:

- FAST OUT input parameter,
- Single mode unchecked
- Threshold level equal to $V_{\rm thr}$
- 8ns Threshold width



Figure 65: lowest trigger threshold to trigger on an event

In our example, V_{thr}=0.6 mV.

Step 6: Take the opportunity to fill in "Dynamic BLR Threshold" with this level V_{thr} =0.6 mV, as explained in § p21.



Figure 66: Dynamic baseline restorer threshold configuration

- ▲ After this BLR threshold, you do not have to change the "Dynamic BLR" Threshold parameter, except if you change the "Fast Out" shaping time. In that case, start over the step 5
- **<u>Step 7:</u>** If better, you can increase "Trigger Threshold Width".

Trigger	Threshold 🛁	Input Fast Out 🛛 🛁	Single mode
	Threshold '2D' :	Level (mV) 0.599	Width 24 ns 🖃

Figure 67: "Trigger module" Threshold '2D' parameters

Depending on the lowest energy you want to detect, you can change "Trigger Threshold Level" as you wish.

IV.D "Out" module parameter definition

Step 8: Preliminary inspect the "Subtraction" signal with Oscilloscope. You will be able to define an approximate baseline level, and the Pole-Zero Cancellation parameter.

In order to inspect the "Subtraction" signal, tune the oscilloscope parameters as shown on Figure 68, i.e.:

- Oscilloscope input: Input Subtraction;
- Time fullscale 1.4 ms or less depending on charge preamplifier time constant;
- Y-fullscale: +/- 2400 mV fullscale for CARAS, and the greatest proposed fullscale for MOSAHR;
- Average parameter: unchecked.
- Delay: 25%.

You can choose 1Hz oscilloscope output frequency, and check "Single mode" if you prefer.

Then, put the "Baseline level" in the "Subtraction" section to zero. The obtained signal will be the same as signal after the "Polarity tuning" module (refer to Figure 6).

CRRC4_SPEC	TRO_1 vert enabled
Input	BNC 1
Subtraction	Base line level (mV) 0.0
Fast Out	Shaping Time 📀 25ns 🗠 60ns
Spectro Out	Shaping 2 µs → Pole-Zero(µs) 500.0 Unipolar → Dynamic BLF → HighFc Thr(mV) 0.595 Gate(µs) 22.095
Trigger	Threshold Input Fast Out Imput Fast Out Single mode Threshold '2D' : Level (mV) 0.599 Width 24 ns Imput Past Out
ADC	Input Spectro Out
Oscilloscope X : Y :	Input Subtraction → □ Without trig. fullscale 1.4 ms → Delay 25% → output +/- 2400 m\→ □ average
Output	ADC 1 7 Counter 1001 7 Oscillo 2001 1 Hz 10 Hz

Figure 68: Oscilloscope tunings to inspect "Offset Subtraction" signal

Thanks to your "Subtraction" signal analysis, you can note:

- An approximate baseline level of the shaper input signal. Report this value in the "Subtraction baseline level" parameter.



Figure 69: Subtraction parameter selection

- An approximate time constant of the charge preamplifier. Report this value in the "Spectro Pole-Zero parameter". You must select "Constant BLR" to enable the Pole-Zero setup.



Figure 70: Pole-Zero cancellation parameter selection.

Step 9: Pre-select the shaping time of the "Spectro Out" Module seems to provide a good spectrum accuracy. For example, select the 1µs shaping time.



Figure 71: Shaping time parameter



Figure 72: Spectrum example.

A You should display with an adequate spectrum resolution. If not, change the spectrum display parameters in RHB -r. Refer to the RHB User Manuel.

Step 10: Re-adjust the Pole-Zero parameters. This time, inspect the "Spectro Out" Signal with the oscilloscope whose setup is described above:

- Oscilloscope input: Spectro Out Signal;
- Time fullscale 1.4 ms or less depending on charge preamplifier time constant;
- Y-fullscale: +/- 37 mV fullscale for CARAS, and the smallest proposed fullscale for MOSAHR;
- Average parameter: unchecked.
- Delay: 25%.



Figure 73: correct compensation

Step 11: Re-adjust the "Constant baseline level" parameter by adding the offset read on the "Out" waveform.



Figure 74: Add baseline level to parameter level

<u>Step 12</u>: Enable the Dynamic BLR, which provides a best spectrum accuracy.

- the Dynamic BLR Threshold has ever been adjusted in step 5;
- Uncheck the "HighFc" parameter if possible for a best accuracy;
- Check the "Auto" parameter, so that the "Gate" parameter will be always adjusted regardless out the shaping time selection.



Figure 75: Dynamic baseline restorer parameters selection

Step 13: Select the best shaping time on the section "Spectro Out", by analyzing the standard deviation of the spectrum peak on the spectrum display.



Don't forget to use the RHB tools to determine the spectrum peak resolution.

Figure 76: RHB tools.

▲ You should avoid the piled-up data for good analysis. Don't forget you can suppress the piled-up data in your spectrum display, by adding a condition (using pile-up flag) on the RHB processing.

In our example, the best parameters are shown on Figure 77:



Figure 77: Selected parameters

Here is your desired spectrum:



Figure 78: ¹³⁷Cs spectrum

<u>Step 14:</u> Click on the "Save" button to prevent from loss of your settings.